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Antenna and RF

Design considerations and challenges of integrating on-chip antennas in nanoscale CMOS technology at millimeter-wave (mm-wave) to achieve a compact front-end receiver for 5G communication systems. Solutions to overcome these challenges are offered and realized in digital 28-nm CMOS. A monolithic on-chip antenna is designed and optimized in the presence of rigorous metal density rules and other back-end-of-the-line (BEoL) challenges of the nanoscale technology. The proposed antenna structure further exploits ground metallization on a PCB board acting as a reflector to increase its radiation efficiency and power gain by 37.3% and 9.8 dB, respectively, while decreasing the silicon area up to 30% compared to previous works. The antenna is directly matched to a 2-stage LNA in a synergetic way as to give rise to an active integrated antenna (AIA) in order to avoid additional matching or interconnect losses. The LNA is followed by a double-balanced folded Gilbert cell mixer, which produces a lower intermediate frequency (IF) such that no probing is required for measurements. The measured total gain of the AIA is 14 dBi. Its total core area is 0.83 mm^2 while the total chip area, including the pad frame, is 1.55×0.85 mm^2.

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