Ongoing developments and plans for low-frequency digital receiver platforms

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Credit: Dorje Angchuk

ARDRA Meeting, Lonavala
15 November 2019

Ongoing digital receiver activities at RRI

RRI is working towards the goal of building precision, high dynamic-range digital receivers for detecting signals from the Epoch of Recombination & the Epoch of Reionization (http://www.rri.res.in/DISTORTION/)

- **SARAS**
  - Detect 21-cm signal from **CD/EoR** in the frequency range 40 to 200 MHz

- **PRATUSH**
  - Radiometer to detect and measure the global 21-cm global signal from CD/EoR (**far-side of the moon**, in a lunar-orbit)

- **APSERa**
  - **A**rray of **P**recision **S**pectrometers for the **E**poch of **R**ecombin**a**tion
  - Detect recombination lines from the Epoch of Cosmological **Recombination** in the frequency range 2 to 6 GHz

SWAN - Indian **S**ky **W**atch **A**rray **N**etwork
http://www.rri.res.in/SWAN/Strategic_Initiatives.html

SARAS experiment

- **SARAS -** (**S**haped **A**ntenna measurement of the background **RA**dio **S**pectrum), a radiometer **purpose designed** to detect the global 21-cm signal from CD/EoR in the frequency range 40-200 MHz
- Every sub system, from the receptor to the digital backend receiver, requires **careful engineering.** The design avoids any spectral features from the receiver system so as to avoid confusing the signal
- **SARAS** experiment involves continuous development, deployment and improvements of the frequency-independent antennas, self-calibratable analog receiver and **digital correlation spectrometer**
  - **SARAS 1 - (87.5 -175 MHz, Patra et al. 2012, Raghunathan et al., 2012)**
  - **SARAS 2 - (110 – 200 MHz, Singh et al. 2018)**
  - **SARAS 3 – (40-100 MHz, ongoing)**
    on a lookout for a freshwater lake in radio-quiet zone

RRI's Digital Signal Processing platform (pSPEC)

Direct RF-sampling ADC and modern FPGA technology allows development of broadband precision receivers

- 2, quad-core 10-bit ADCs (EV10AQ190 from e2V)
- Time-interleaving of 2 cores/4 cores
- F_{clk} =1.25/2.5/5 GSPs, ABW=3.2 GHz
- Xilinx Virtex 6 LX240T or SX315T FPGA
- GigE , 4 Gbps optical fiber links **(**FTLF 1324P2BTL **)**
- Quad SFP module**:** AFBR-79Q4Z (40 Gbps)

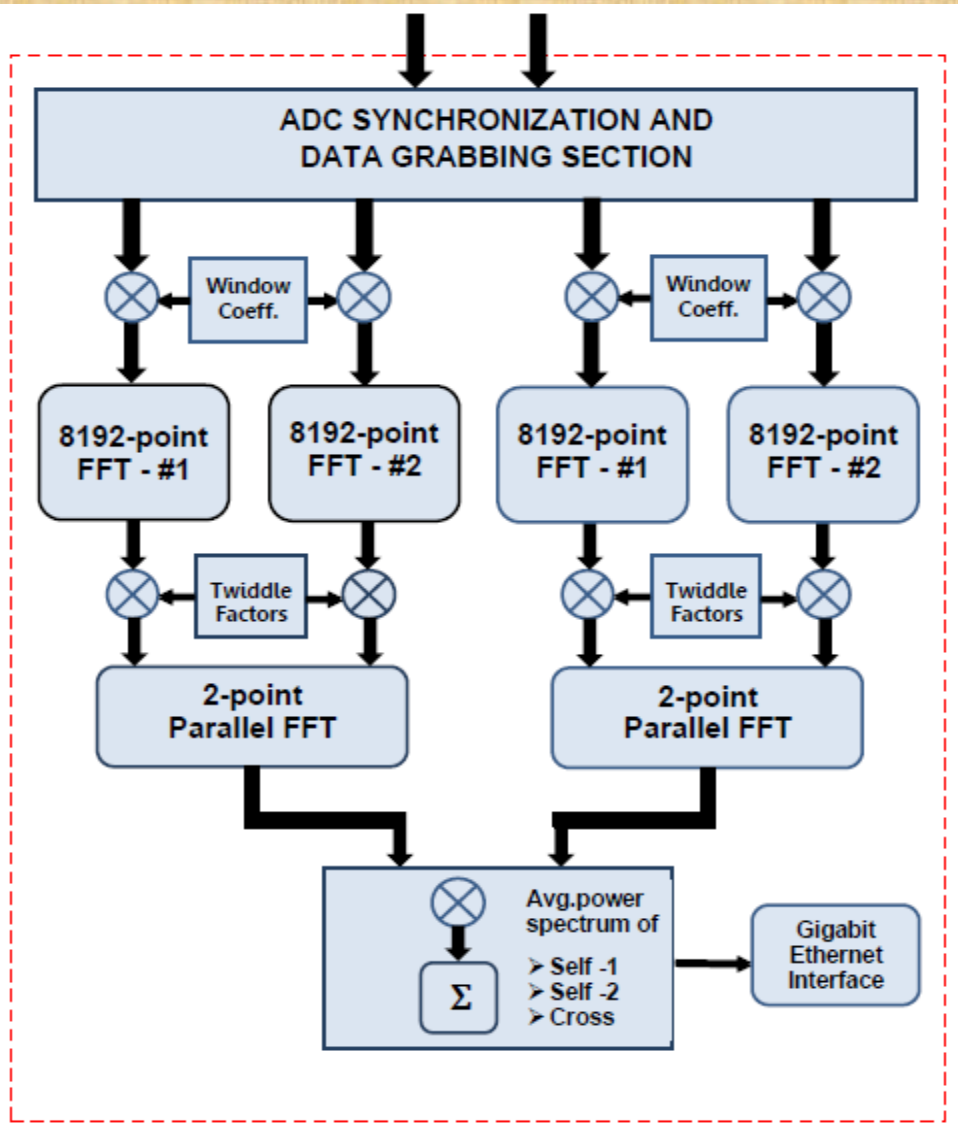
- Fully designed & developed at RRI
- Fabrication of 18-layer PCB with controlled impedance traces and special dielectric material for high frequency traces – by a local industry at Bengaluru
- Assembly of 1156-pin BGA package carried out by another industry in Bengaluru, with X-ray imaging capability for PCB assembly process(for quality assurance)

Digital Correlation Spectrometer

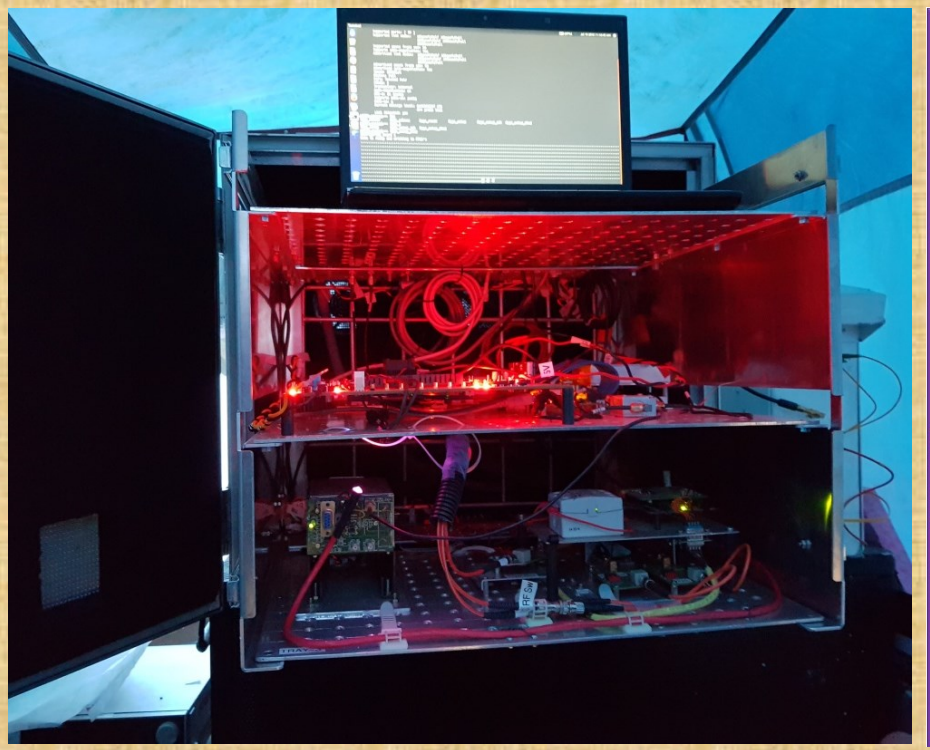
- Optimized VHDL firmware for ADC data grabbing and real-time F-X correlation inside Virtex 6 FPGA has been developed

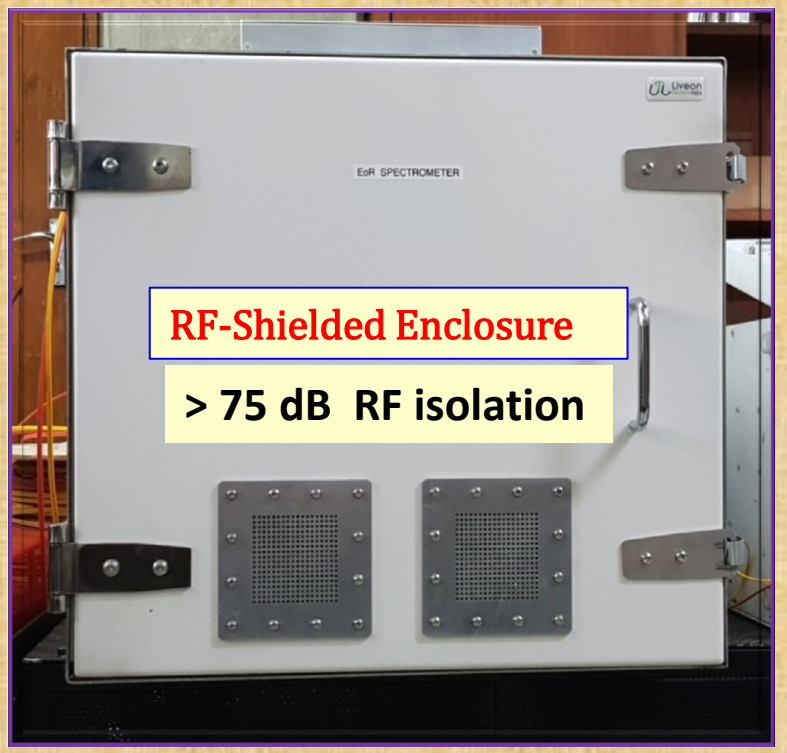
Spectrometer Parameter	Value
Analog inputs, BW	2, 40-200 MHz band
Sampling speed	500 MSps
Window function	4-term Blackman-Nuttal
Length of FFT	16,384 points
Spectral resolution	~ 61 kHz
On-chip integration	~ 67 ms
Output	Avg. power spectrum • Self-power & •Cross-power

FPGA Resource utilization	Usage	Percentage
Number of occupied slices	9478 out of 37680	25
Number of RAM36E1	236 out of 416	56
Number of MMCM	6 out of 12	50
I/O	191 out of 600	31
Number of DSP48E1s	114 out of 768	14
Number of TEMACs	1 out of 4	25



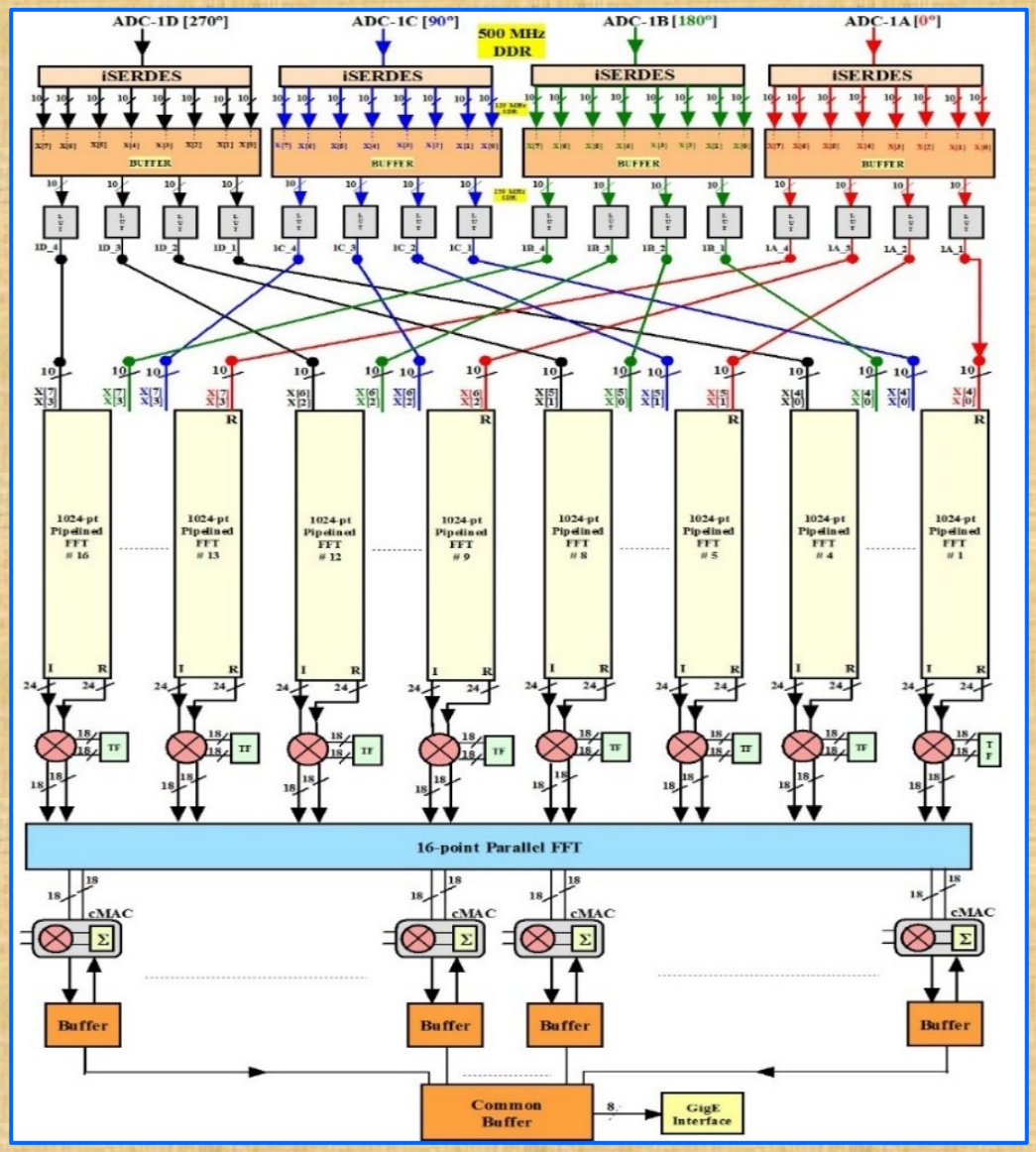
Integrated SARAS 3 Spectrometer - ready for deployment





- **High resolution**, high **dynamic-range** digital correlation spectrometer has been designed, developed and assembled inside an RF-Shielded
- A side lobe suppression of **~80 dB**; helps in limiting the deleterious effect of RFI affected spectral channel
- Compact, portable, easily deployable and operates off internal batteries

FPGA Signal Processing for wide bandwidth applications (APSERa)



- Synchronization of multiple ADC cores
- OGP calibration of time-interleaved ADC cores
- Digitization (BW =2 GHz @ 4GSps)
- 1024-point FFT channelization
- Correlation Spectrometer
- Self- and cross-power spectrum
- Monitor and Control interface
- Complex FPGA firmware design to meet timing closures (250MHz)
- 2 bands, each of BW=2GHz is processed inside a Virtex 6 SX315T FPGA

PRATUSH (beginning of day; dawn in Sanskrit)

Probing **R**eioniz**AT**ion of the **U**niverse using **S**ignal from **H**ydrogen

- Equivalent of SARAS, but, space-based
- A precision radiometer to detect and measure the redshifted global 21-cm signal from CD/EoR in the frequency range 40-200 MHz
- In a lunar-orbit; radio-quiet environment on far-side of the moon
- The **I**ndian **S**pace **R**esearch **O**rganization (ISRO) has provided funding for pre-project activities for 2019-20

Among other things, we have the following deliverables:

- Antenna that can be deployed in space
- A compact, calibratable analog receiver
- Digital spectrometer
- Orbit

Why space (far-side of moon)?

- Terrestrial RFI
- Ionosphere
- Confusion from antenna interaction with the inhomogeneous Earth over which antenna is placed

PRATUSH digital receiver

- We are working on the design of a digital receiver for PRATUSH with focus on reducing SWaP attributes (Size, Weight and Power)
- We have shortlisted a few space-grade ADCs and Kintex UltraScale FPGA XQRKU060, and working on the design of a hardware platform around these devices
- In parallel, we are developing spectrometer firmware in VHDL targeting XQRKU060 using Xilinx Vivado Design Suite

	XQRV4QV	XQRV5QV	XQRKU060
Radiation Hardness	Tolerant	Hard	Tolerant
Process (nm)	90	65	20
Memory (Mb)	4.1 to 9.9	12.3	38
System Logic Cells (k)	55 to 200	131	726
MGTs	None	18 at 3.125 Gbps	32 at 12.5 Gbps
User I/O	640 to 960	836	620
DSP Slices	32 to 192	320	2,760

Source: Kintex Ultrascale FPGAs for Space Applications – Rajan Bedi, 15 March 2019

Ahead of previous space-grade FPGA (V4 and V5) in terms of bandwidth, high throughput on-board processing, capacity, etc

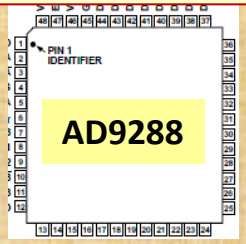
ADCs @ RRI over the years…

Complexity

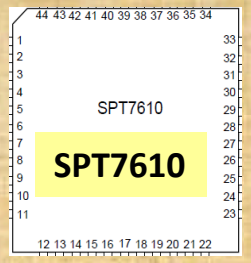
- ADCs moving from (**big A, small D**) in the 1990s and 2000s to (**small A, big D**)
- RF-sampling ADCs packed DDC with down sampling, DeMux, DAC, Serializers

50 MHz @GMRT

8- bit
80 MSps
ABW=0.475 GHz



6-bit ADC
1GSps
ABW=1.4 GHz



@ RRI

8- bit
1 GSps
ABW=1.5 GHz

MWA-1

10- bit
1.25/2.5/5 GSps
ABW=3.2 GHz

SARAS
APSERa
SWAN

4- bit
15 GSps
ABW=20 GHz

RRI

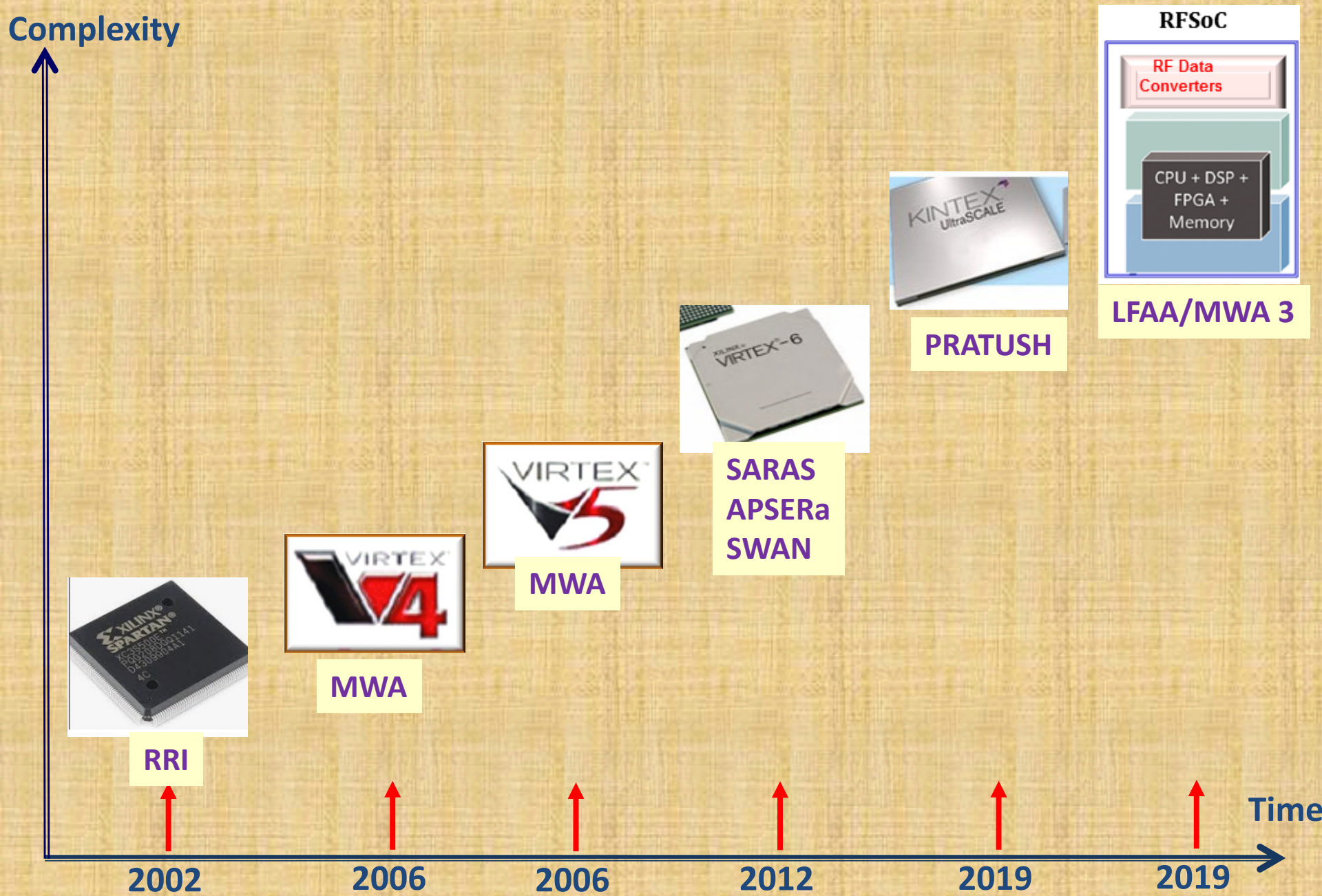
12- bit
4 GSps
ABW=4 GHz

LFAA?

Time

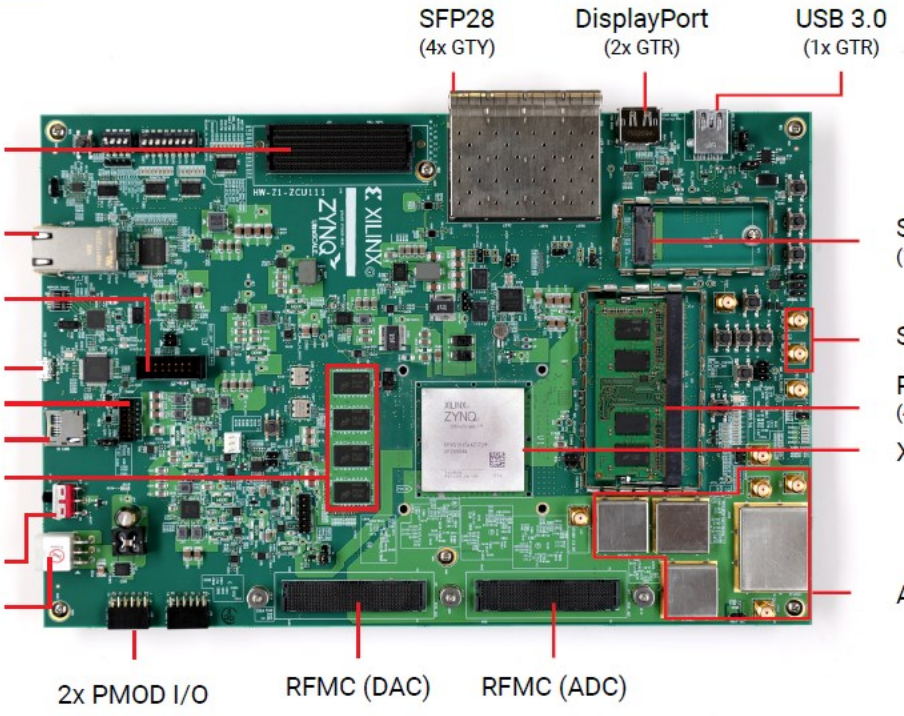
2004 **2005** **2006** **2012** **2016** **2019**

Xilinx FPGAs at RRI over the years…



ZCU111 – At RRI, implementing SARAS Correlation Spectrometer

ZCU111 Evaluation Board



Part Number: EK-U1-ZCU111-G

- **11.31" x 7.87"**
- **2.56 mm thick**
- **18-layer stack up**

Picture from ZCU111-product-brief.pdf

- XCZU28DR-2FFVG1517E RFSoC integrated with 8x4GSPS 12-bit ADCs, 8x 6.5GSPS 14-bit DACs, and 8 SD-FECs
- DDR4 Component – 4GB, 64-bit, 2666 MT/s, attached to Programmable Logic (PL)
- DDR4 SODIMM – 4GB, 64-bit, 2400 MT/s, attached to Processor Subsystem (PS)
- Ganged SFP28 cage to support up to 4 SFP/SFP+/zSFP+/SFP28 modules
- 10/100/1000 based Ethernet support over RGMII PHY to RJ-45 connector
- USB3, DisplayPort, and SATA
- 2x PMOD connectors
- FMC+ connector
- RFMC ADC and DAC connectors

- Zynq UltraScale+ RFSoC ZCU111 Evaluation Board
- XM500 RFMC balun transformer add-on card
- 6 filters (two 2500 MHz low pass, two 1300 MHz low pass, two 3000-4300 MHz bandpass)
- Cables (6 SMAs, USB, Ethernet, Power)
- Xilinx Vivado Design Suite Node/Device-Locked License with 1 year of updates
- Access to Analog-Mixed Signal (AMS) Reference Design
- Additional hardware (MicroSD, tools)
- Quick Start Guide

Zynq UltraScale+ RFSoC Product Table

	Device Name	ZU21DR	ZU25DR	ZU27DR	ZU28DR	ZU29DR	ZU39DR	ZU43DR	ZU46DR	ZU47DR	ZU48DR	ZU49DR
				Gen 1			Gen 2			Gen 3		
PS		Quad-core Arm® Cortex™-A53 MPCore™ up to 1.3GHz, Dual-core Arm Cortex-R5 MPCore up to 533MHz										
RF Data Converter	12-bit RF-ADC w/DDC # of ADCs	0	8	8	8	16	16	–	–	–	–	–
	12-bit RF-ADC w/DDC Max Rate (GSPS)	0	4.096	4.096	4.096	2.058	2.220	–	–	–	–	–
	14-bit RF-ADC w/DDC # of ADCs	–	–	–	–	–	–	4	8 4	8	8	16
	14-bit RF-ADC w/DDC Max Rate (GSPS)	–	–	–	–	–	–	5.0	2.5 5.0	5.0	5.0	2.5
	14-bit RF-DAC w/DUC # of DACs	0	8	8	8	16	16	4	12	8	8	16
	14-bit RF-DAC w/DUC Max Rate (GSPS)	0	6.554	6.554	6.554	6.554	6.554	10.0	10.0	10.0	10.0	10.0
	SD-FEC	8	0	0	8	0	0	0	8	0	8	0
	Number of DDCs per RF-ADC[1]	0	1	1	1	1	1	2	1	1	1	1
	RF input Freq max. GHz			4			5			6		
	Decimation / Interpolation			1x, 2x, 4x, 8x			1x, 2x, 4x, 8x	1x, 2x, 3x, 4x, 5x, 6x, 8x, 10x, 12x, 16x, 20x, 24x, 40x				
Programmable Logic (PL)	System Logic Cells (K)	930	678	930	930	930	930	930	930	930	930	930
	CLB LUTs (K)	425	310	425	425	425	425	425	425	425	425	425
	Max. Dist. RAM (Mb)	13.0	9.6	13.0	13.0	13.0	13.0	13.0	13.0	13.0	13.0	13.0
	Total Block RAM (Mb)	38.0	27.8	38.0	38.0	38.0	38.0	38.0	38.0	38.0	38.0	38.0
	UltraRAM (Mb)	22.5	13.5	22.5	22.5	22.5	22.5	22.5	22.5	22.5	22.5	22.5
	DSP Slices	4,272	3,145	4,272	4,272	4,272	4,272	4,272	4,272	4,272	4,272	4,272
	GTY Transceivers	16	8	16	16	16	16	16	16	16	16	16
	PCIe® Gen3 x16	2	1	2	2	2	2	–	–	–	–	–
	PCIeGen3 x16/Gen4 x8 / CCIX[2]	–	–	–	–	–	–	2	2	2	2	2
	150G Interlaken	1	1	1	1	1	1	1	1	1	1	1
	[illegible]	[illegible]	[illegible]	2	2	2	2	2	2	2	2	2
	[illegible]	[illegible]	[illegible]	1	1	1	1	1	1	1	1	1
	[illegible]	[illegible]	[illegible]	-1E, -1I, -1LI, -2E, -2LE, -2I, -2LI	-1E, -1I, -1LI, -2E, -2LE, -2I, -2LI	-1E, -1I, -1LI, -2E, -2LE, -2I, -2LI	-2I, -2LI	-1E, -1I, -1LI, -2E, -2I, -2LI	-1E, -1I, -1LI, -2E, -2I, -2LI	-1E, -1I, -1LI, -2E, -2I, -2LI	-1E, -1I, -1LI, -2E, -2I, -2LI	-1E, -1I, -1LI, -2E, -2I, -2LI
	[illegible]	[illegible]	[illegible]	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC	PSIO, HDIO, HPIO GTR, GTY RF-ADC, RF-DAC
	[illegible]	[illegible]	[illegible]									
E1156	35x35		214, 48, 104 4, 8 8, 8	214, 48, 104 4, 8 8, 8	214, 48, 104 4, 8 8, 8			214, 48, 104 4, 8 4, 4		214, 48, 104 4, 8 8, 8	214, 48, 104 4, 8 8, 8	
G1517	40x40		214, 48, 299 4, 8 8, 8	214, 48, 299 4, 16 8, 8	214, 48, 299 4, 16 8, 8			214, 48, 299 4, 16 4, 4		214, 48, 299 4, 16 8, 8	214, 48, 299 4, 16 8, 8	
F1760	42.5x42.5					214, 96, 312 4, 16 16, 16	214, 96, 312 4, 16 16, 16					214, 96, 312 4, 16 16, 16
H1760	42.5x42.5								214, 48, 312 4, 16 12, 12			

1. This value applies when all RF I/O of an RF-ADC tile are used.
2. This block operates in compatibility mode for 16.0GT/s (Gen4) operation. See PG213.

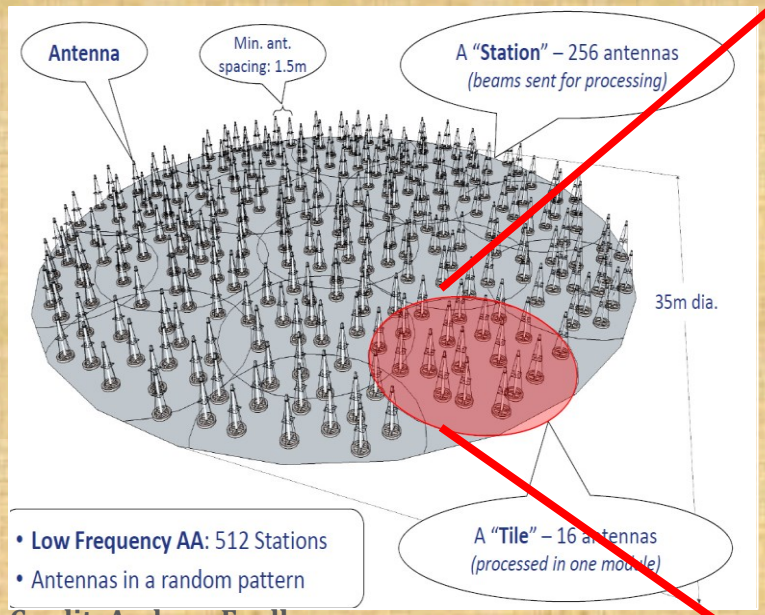
XILINX

Zynq® UltraScale+™ RFSoCs

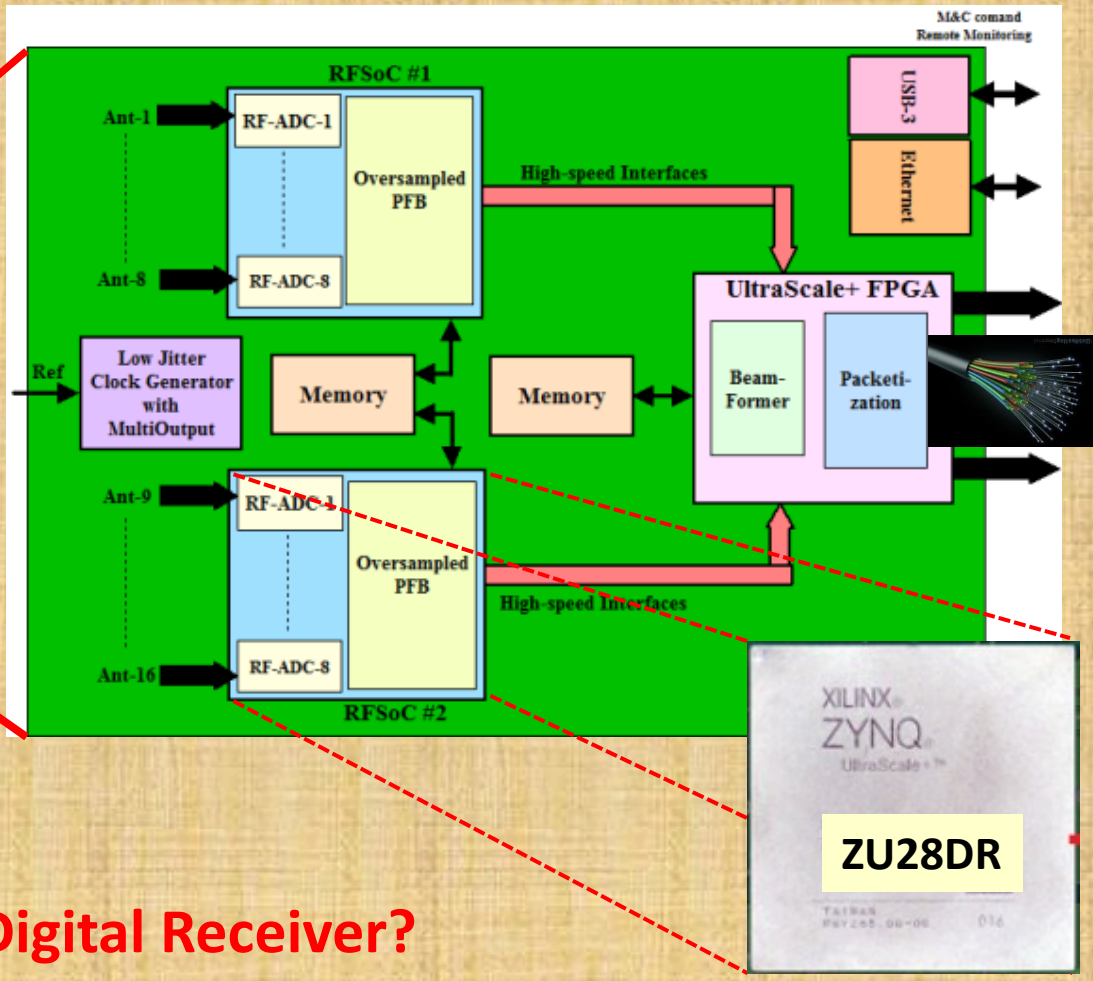
Q1 2020

We have a ZCU111 Evaluation board @ RRI (SARAS correlation Spectrometer)

Artist impression of the core of the first-stage digital receiver for MWA 3/LFAA



Credit: Andrew Faulkner



Suitability to LFAA /MWA 3 Digital Receiver?

- Digitization + Channelization + Beam forming + Packetization
- 2 such DSP platforms for 16 antennas (dual Pol) in an SKA Tile
- **32** such platforms for an SKA station
- 32/station x**512** stations = **16384** such platforms for **131072** LFAA antennas

Summary and Conclusions

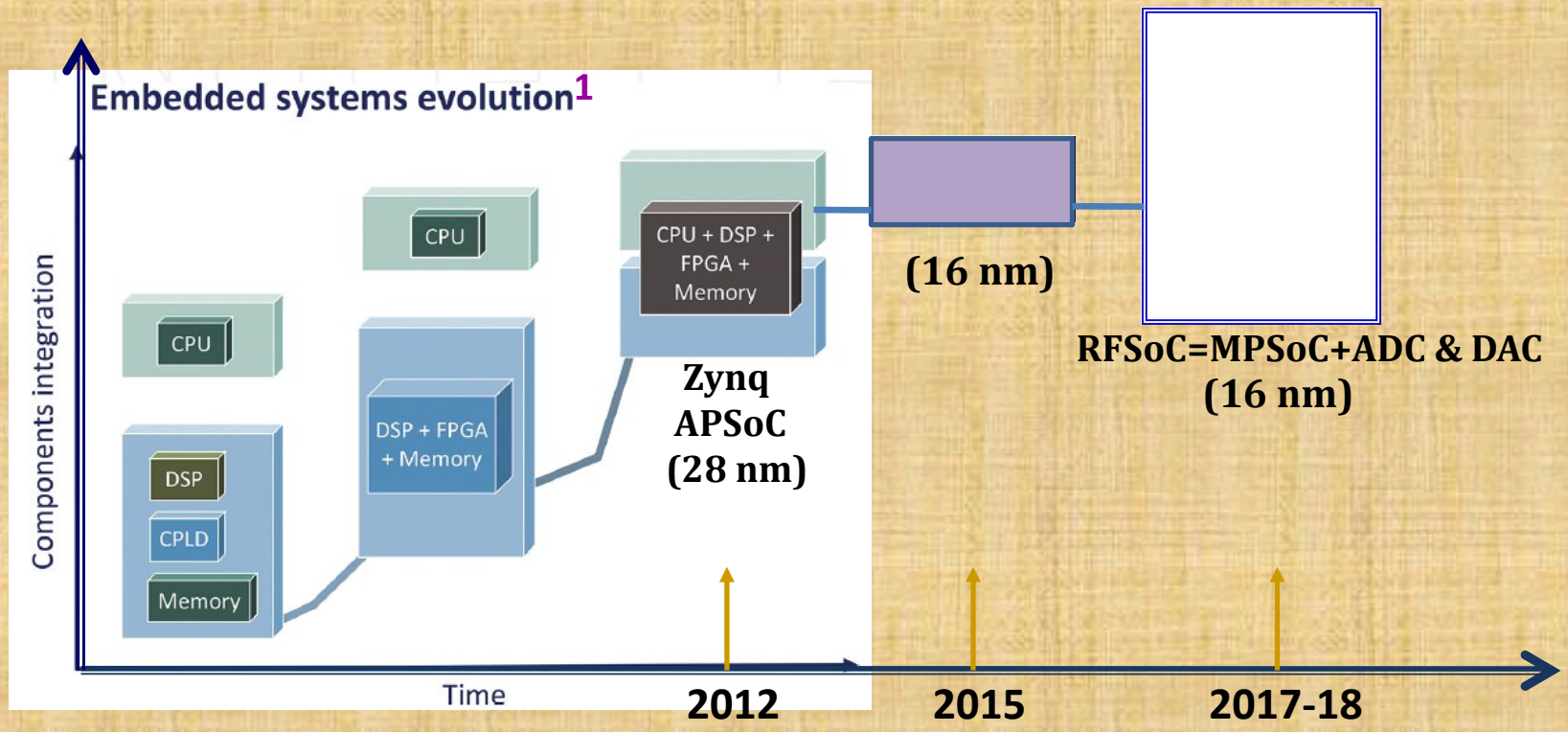
- RFSoCs are meant for massive Multiple-Input, Multiple-Output (M-MIMO) requirement
- Looks like RFSoC is the way-forward for designing next-generation digital receivers for large N radio astronomy applications (LFAA/MWA 3)
- It is claimed that RFSoCs reduce physical footprint, power consumption by **50-75**%
- A platform consisting of 2 RFSoCs would be capable of digitizing and processing 16 (single Pol) analog inputs.
- When scaled to LFAA requirements, there are advantages to be gained in terms of reduction in BoM, power, physical footprint and cooling requirements.
- **At the Raman Research Institute, we have a demonstrated expertise in development of signal processing platforms with state-of-the-art ADCs & FPGAs for low-frequency radio astronomy**
- **Includes hardware, firmware and algorithms inside FPGA**
- **Happy to collaborate in the development of DR, DSP**

SARAS and PRATUSH team at RRI

- Ravi Subrahmanyan
- Girish B. S.
- Jishnu Nambissan T.
- Mayuri Sathyanarayana Rao
- Raghunathan A.
- Saurabh Singh
- Somashekar R.
- Srivani K. S.
- Udaya Shankar N.

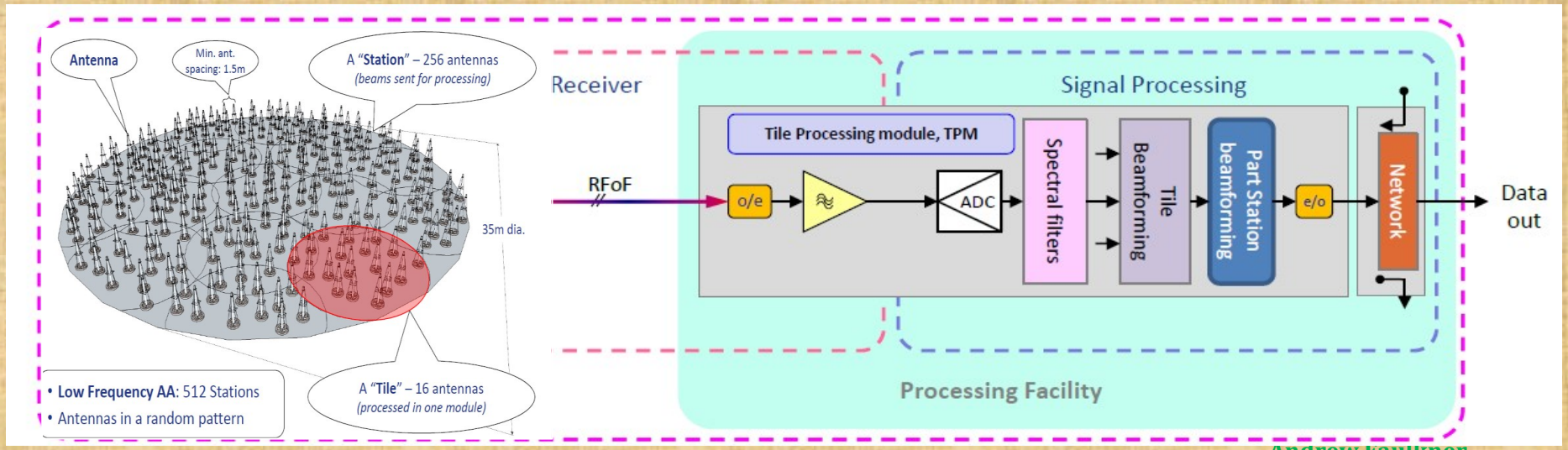
Thanks for your time and attention!

Radio-Frequency System-on-chip (RFSoC) arrives on the scene in 2018



- ADCs morphing from (**big A, small D**) in the 1990s and 2000s to (**small A, big D**) [1]
- RF-sampling ADCs packed with lot more digital processing capability, enhancing the ADC's performance[1] **(DDC with down sampling, DeMux, DAC, Serializers)**
- ADCs do a lot of digital processing in the ADC silicon at speed, and take up some of the digital processing load from the FPGA[1]

1 Design of Digital Advanced Systems Based on Programmable System on Chip, Azanzabal et. al



Andrew Faulkner

Antenna	**Log Periodic , 131,072 (2^{17})**
Ant. Spacing	**1.5m (av. ~1.9m),** 80 km baseline
Frequency	**50MHz – 350MHz and 375-650MHz**
Sampling Clock	**800 MSps, 700 MSps**
Polarisation	**Dual**
Station size	**256 antennas ~40m dia. 512 stations**
Configuration	**75% <2 km radius, remaining 3 spiral arms extending up to 50km**
Channelization	**PFB, ~1 MHz sub bands**
Processing	**Digital, 8-bit**
Data-Rate	**~8Tb/s (total)**

Challenges

- **Digitizing 131,072 antennas**
- **Digital processing/Modelling**
- **Tile & Station beamforming**
- **Large bandwidths/throughput rates**
- **Power , Size and Cost**
- **Mass production, Deployment**
- **Maintenance, Serviceability**
- **Remote site conditions**