Wide Band Digital Tile Processing System for Low Frequency Array

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This talk is partitioned in to 3 segments:

1. Technology development of Digital Receivers at RRI- MWA, SARAS etc

2. Technology development at RRI towards Sky Watch Array Network

3. Possible future technology for future telescopes : SKA, MWA Phase 3

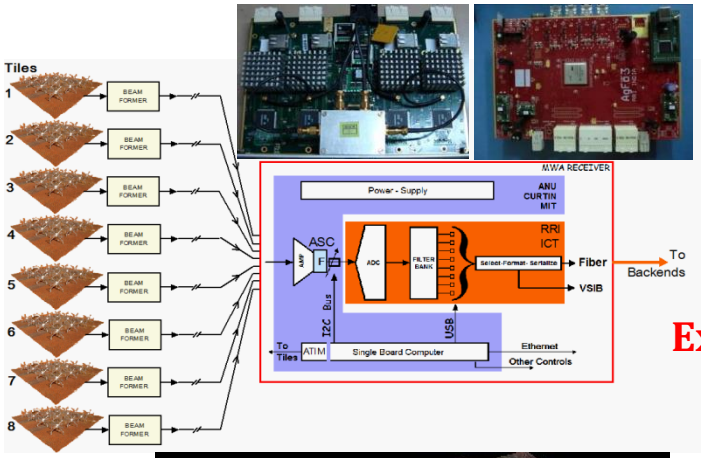
The focus of this talk is on Digital Tile Processors

Technology development of Digital Receivers at RRI

RRI participation: National and International Telescopes

A precursor for the SKA - Murchison Wide Field Array (MWA)

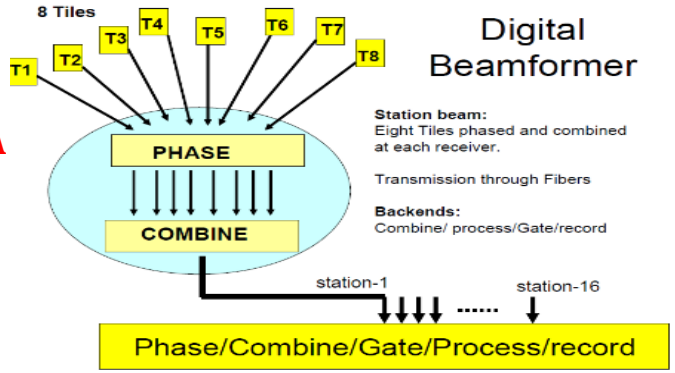
- 2048/4096 dual-pol dipole antennas
- Operates from : 80-300 MHz
- Processed bandwidth : 30.72 MHz



A full 300 MHz bandwidth (PA)mode for pulsar/transient studies at Gauribidanur Radio Observatory(GBD)

- 8 tiles combined at each station
- Final stages of evaluation at GBD
- VCS in hardware
- Multiple Beams – trade-off channels

Existing Ch mode and PA mode set thru s/w registers



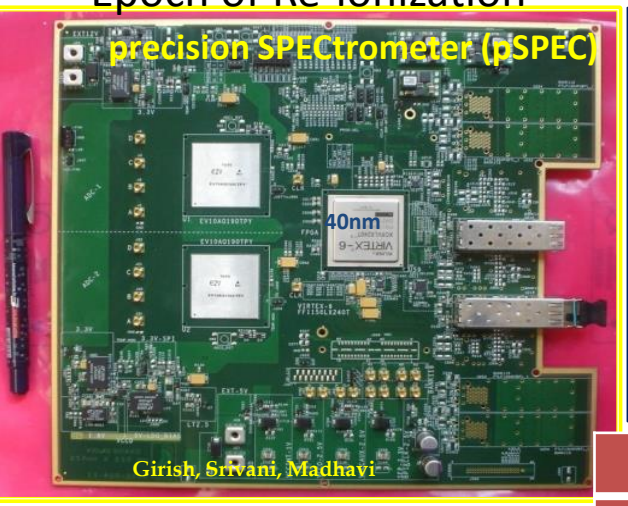
- Digital receivers developed at RRI*
- Active involvement of industry
- Mass production of 16 DRs→ 128 Tiles
- PA mode @ GBD to PA mode @MRO

Prabu, Srivani, Kamini, Madhavi, Goplakrishna ,Anish Roshi, UdayaShankar , Avinash Deshpande and Ravi Subrahmanyan & Collaborators

Spectrometer for DISTORTION experiments

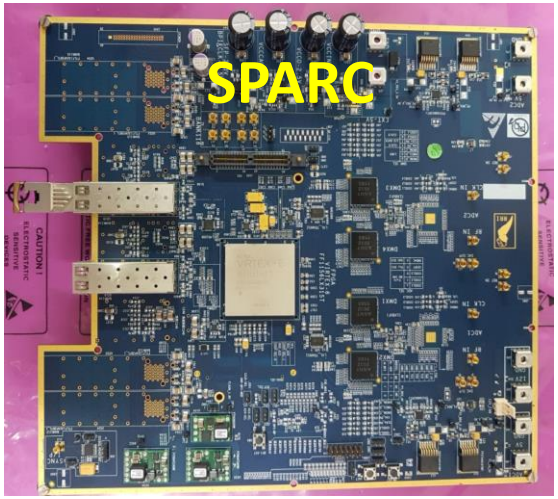
A venture to experimentally verify signatures from the early universe→ Precision Receivers

Epoch of Re-ionization



PRATUSH – Space based venture
Probing ReionizATion of the Universe using Signal from Hydrogen
Kintex-ultrascale space grade FPGA-XQRKU060 and 12/14 bits ADCs

Epoch of Recombination



	SARAS/ APSERa
RF BW range	40 - 250 MHz/2GHz
channelizer	16K / 1K Correlation Spectrometer
On-chip intg	61 ms/16.77ms
Sensitivity	1 part in 10^5 /10^{57}
Power	150W/ 250W
ADC	EV10AQ190CTPY QUAD 10-bit, ABW~3GHz/5 Gsps ASNT7120A- single core , 4-bit ABW~20GHz , Fs: DC-15GSps
FPGA	FPGA : XC6VSX315T

Girish, Srivani ,Ravi Subrahmanyan, UdayaShankar N.

2GHz Hybrid Correlation Spectrometer

- 2 GHz, 8K channels → using GTX1050 and Virtex-6 FPGA in burst mode
- Real-time GPU system using state-of-the-art P100/V100 GPUs and powerful work-station

- Digitization of bandwidth - 250MHz/ 2GHz
- Industry : Fabrication & assembly of boards and RF Shielded Enclosure
- Hardware, Firmware & System development → in-house

Details in Girish Talk

Technology development → The Indian SWAN (Sky Watch Array Network)

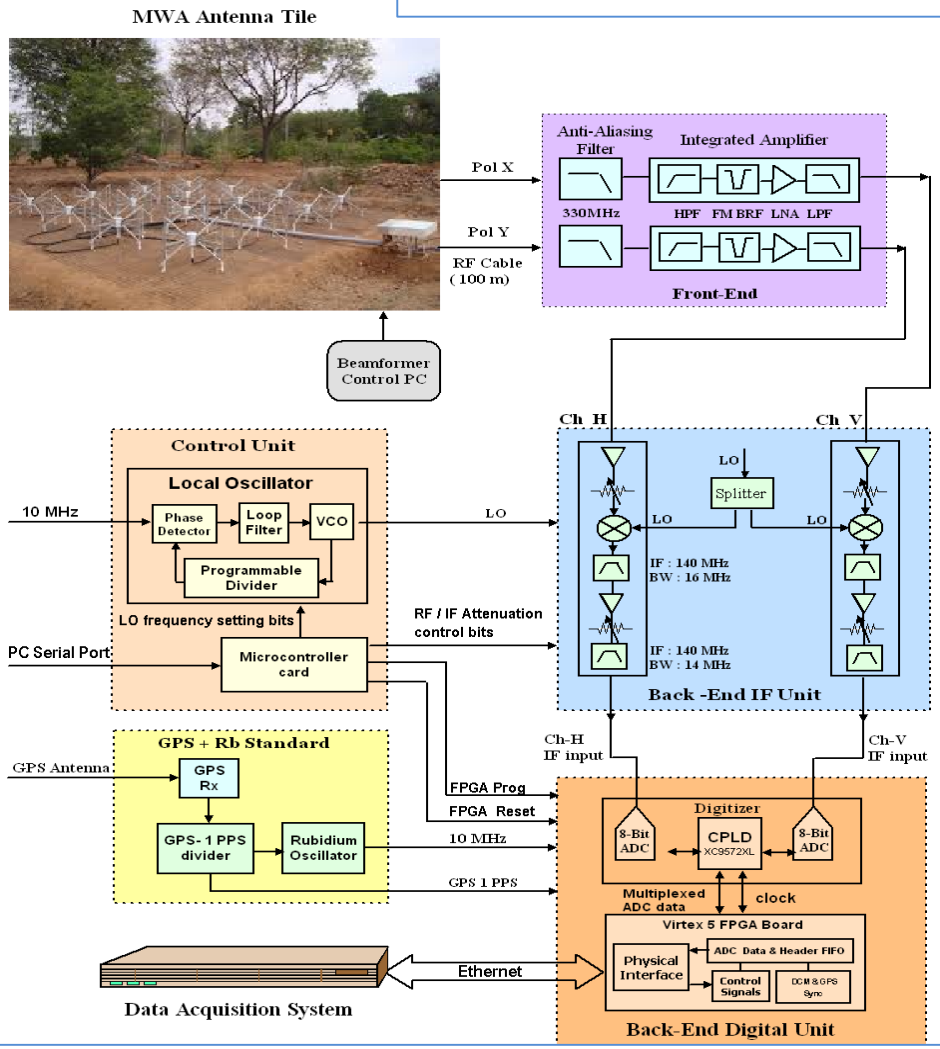
- Science: conduct searches and studies of fast transients, pulsars etc.
- Aim to Enhance Indian observing capabilities in radio
  - Build & nurture future generations of talented radio astronomers in India
  - To facilitate hands-on experience to a large number of students
  - Direct & active participation, starting from design stage to competitive research using SWAN in Desh's talk

- Phase 0 → As a proof-of-concept/demonstrator system:
  - A 7-station system, using small tiles (based on MWA design)
  - Modified Receiver hardware from RRI-GBT Multiband system (MBR) is successfully configured at the Gauribidanur Telescope Field Station
  - The MBR is currently being characterized & tested in a tied-array mode.
  - Eventually the 7-station system will be deployed at various institutes across India.

Team: Vinutha Chandrashekar, K. B. Raghavendra Rao, Rahul Kinger, H. A. Aswathappa, P. S. Sasikumar, T. S. Mamatha [1] Bhawana Bansal, Harsh Grover, H. N. Nagaraja [1] Sandhya [1], Indrajit Barve and A. Deshpande [1]

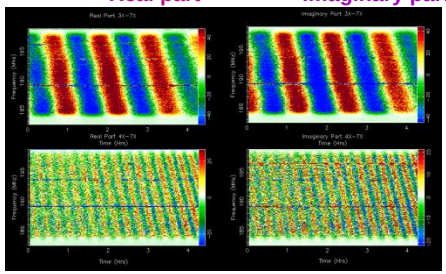
7-Tile Array at Gauribidanur Radio Telescope Observatory- Phase -0

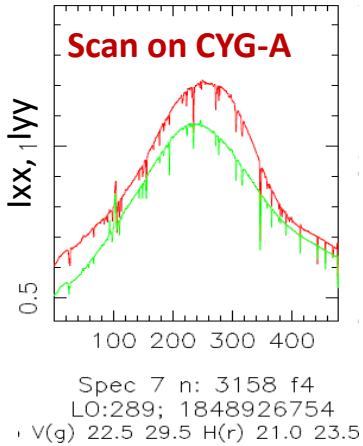
- 15 sq. m aperture (each tile)
- Frequency : 80 – 320MHz
- Bandwidth : 16MHz



Dynamic Spectra of Complex Correlation/Visibility Baselines Tile3-Tile7 (above) , and Tile4-Tile7 (below)

Real part Imaginary part





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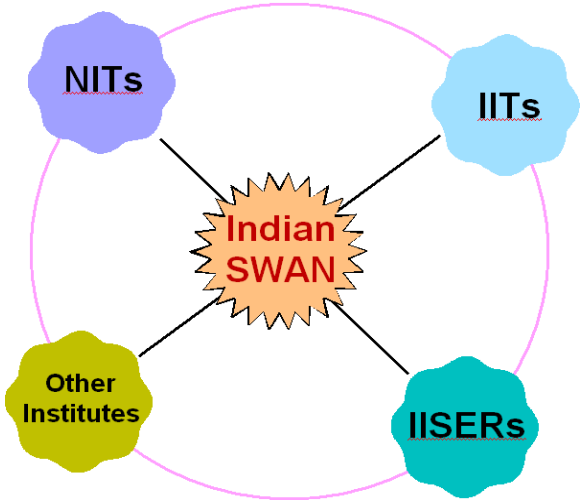
SWAN System configured for Concept Demonstration –Phase 0

- Initiation of a collective effort to develop the SWAN with as many as science institutes i.e. the (IIT, NIT, IISER)s, and some universities across India.
- At present, remote access of the system existing in Gauribidanur radio field station, from respective parent institutions/universities .



Phase 1→

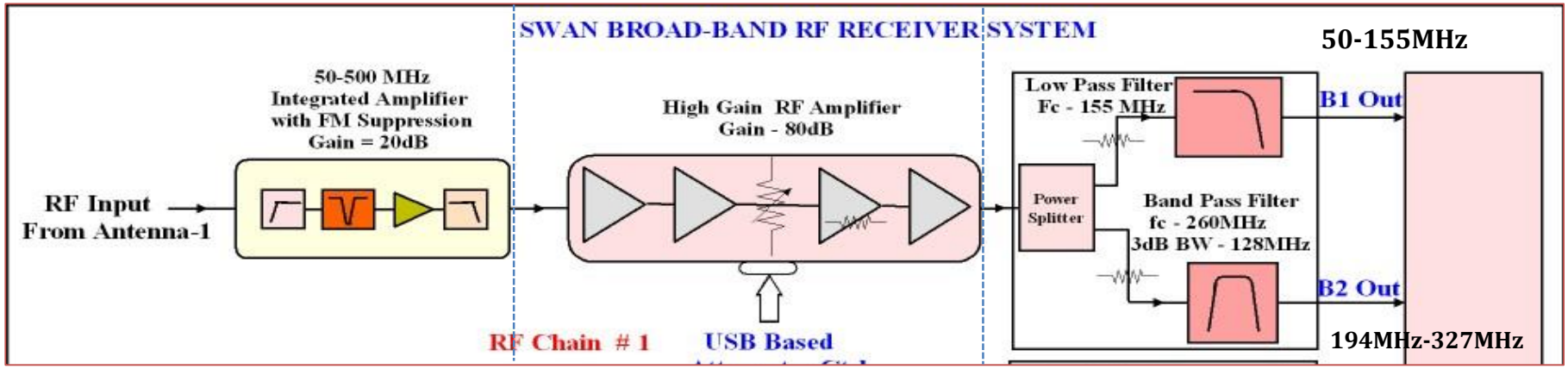
- Design, develop and use a wide-band (50 MHz – 500 MHz)-interferometric array of antenna across different parts of India
- The front-end Rx system can handle four input RF signals without frequency down-conversion.
  - Low noise, high gain receiver chain, capability to reject the FM band and avoid saturation
- Direct digitization with Instantaneous bandwidth of – 175MHz each
- The digital correlator receiver has 8 independent channels with high-speed ADC and Virtex-6 FPGA.

PHASE -1 Receiver System

A wide-band low noise amplifier with FM rejection and first level band limiters

A High gain broad-band RF amplifier

A band-pass micro-strip filter for band shaping the RF signal for further digitization.



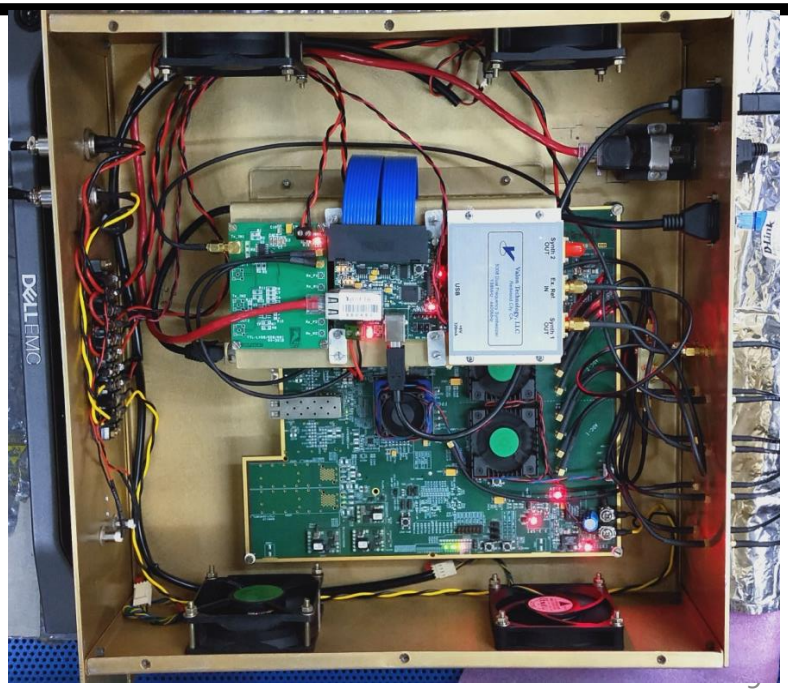
- 4 such chains form wide band receiver system for SWAN
- Designed and built in-house

Phase-1 : Wide Band Digital Tile Processor

An eight input digital receiver consists of :

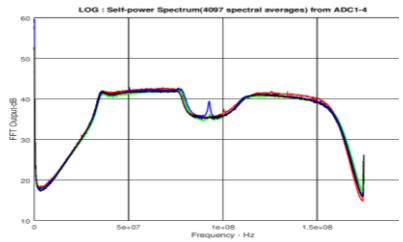
- A general purpose platform consisting of high-speed Quad ADCs and Virtex-6 FPGA forms the Digital backend receiver for SWAN.
- Full Stokes Correlator with 1024 spectral channels over a bandwidth of about 350 MHz

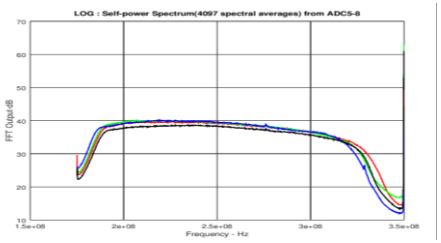
	SWAN Wide Band
RF BW range	5-500MHz
channelizer	2K
On-chip intg	23.87 ms
Power	75W
ADC	EV10AQ190CTPY QUAD 10-bit, ABW~3GHz/5 Gsps
FPGA	FPGA : XC6VLX240T
Spectral Resolution	170 kHz
	Full STOKES correlator
Data-rate	21MBytes/sec

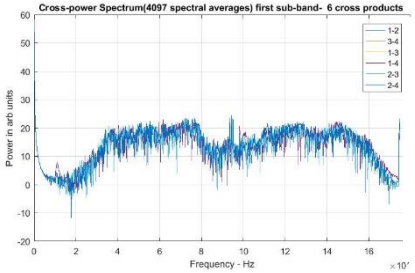


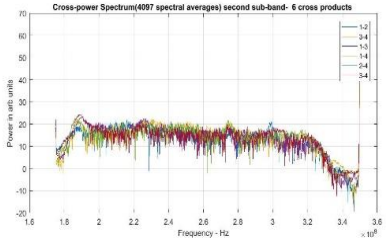
Phase-1 : Wide Band Digital Tile Processor

Rx system sub-band 1 and 2 output









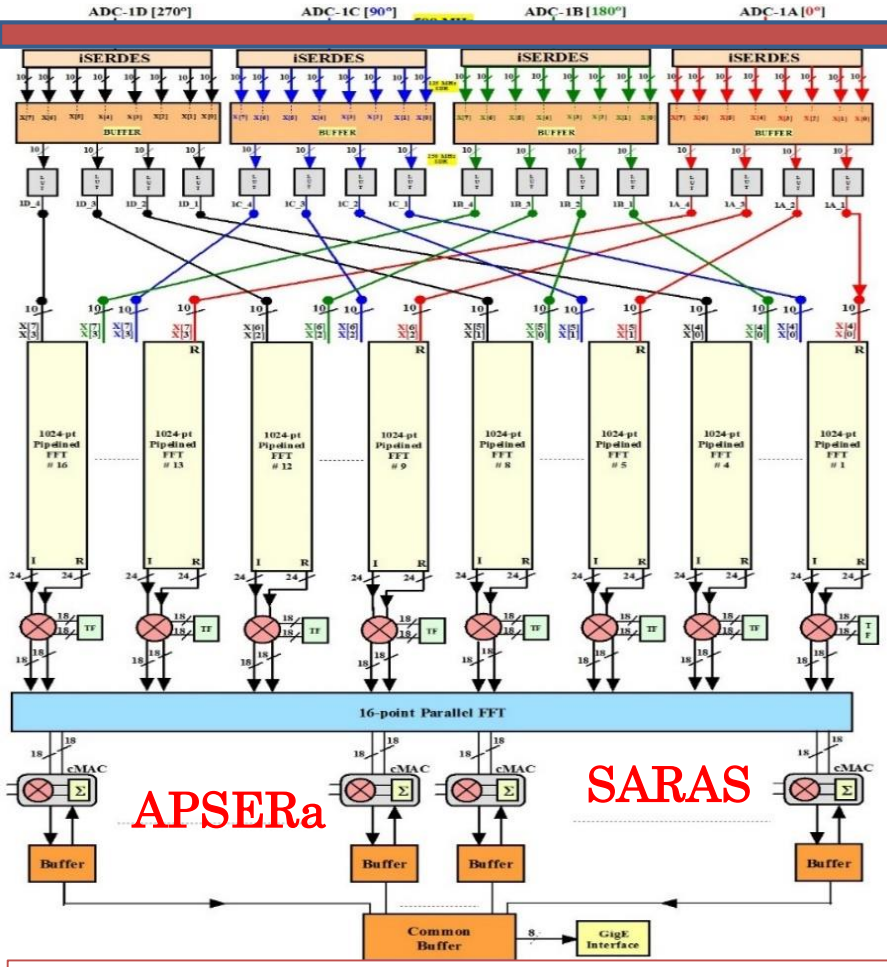
Current Status :

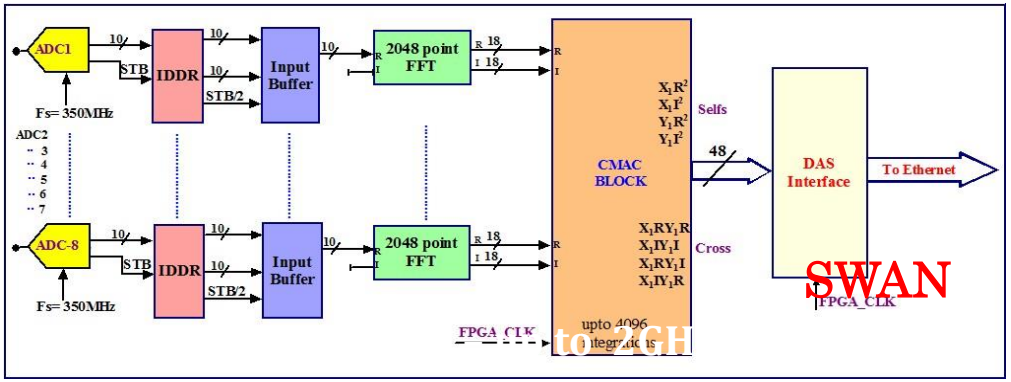
- Laboratory tests with integrated analog receiver is in progress
- Eventually will be interfaced to MWA Tiles @ GBD for sky observations.

Integrated Digital Receiver Front-Rear view

- 24 complex & 8 self products in a single chip
- Resource utilization is less than 50%
- Frequency of operation is 350 MHz
- Can be configured as
  1. 2 antennas dual pol- 375MHz BW
  2. 4 antennas single pol-375 MHz BW
  3. 4 antennas dual pol- 175MHz BW
  4. 8 antennas single pol- 175MHz BW

FPGA signal processing and data packetization architectures



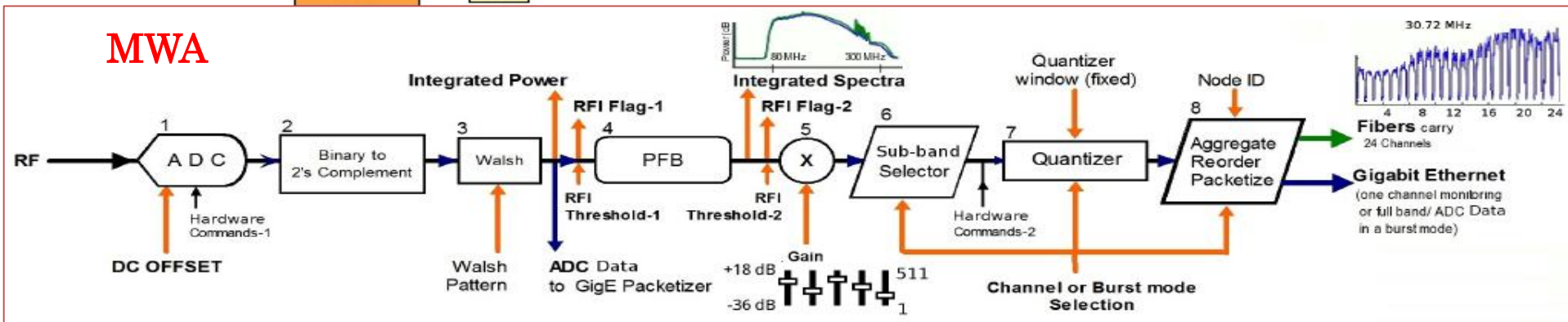


Channelization algorithms

Total power & channelized power detection

Monitor and Control & Optical fiber interface

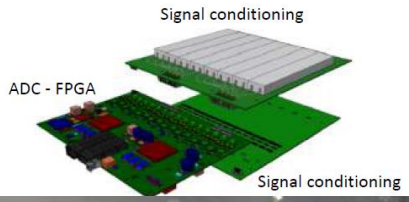
Complex design- Meeting timing closures(163.84MHz, 250MHz, 350MHz) inside FPGAs

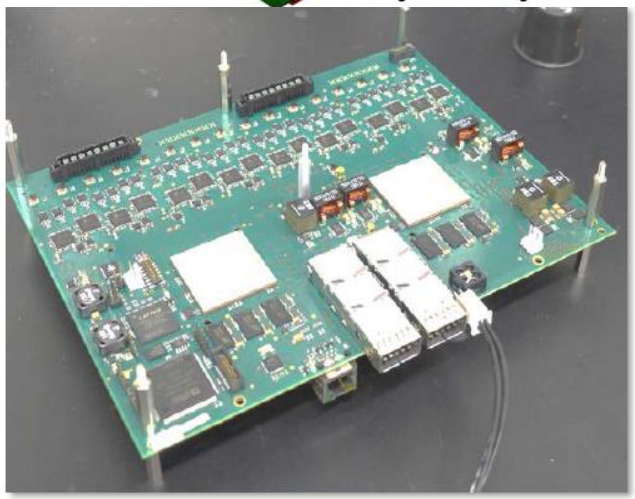


Technology development world wide → LFAA-SKA

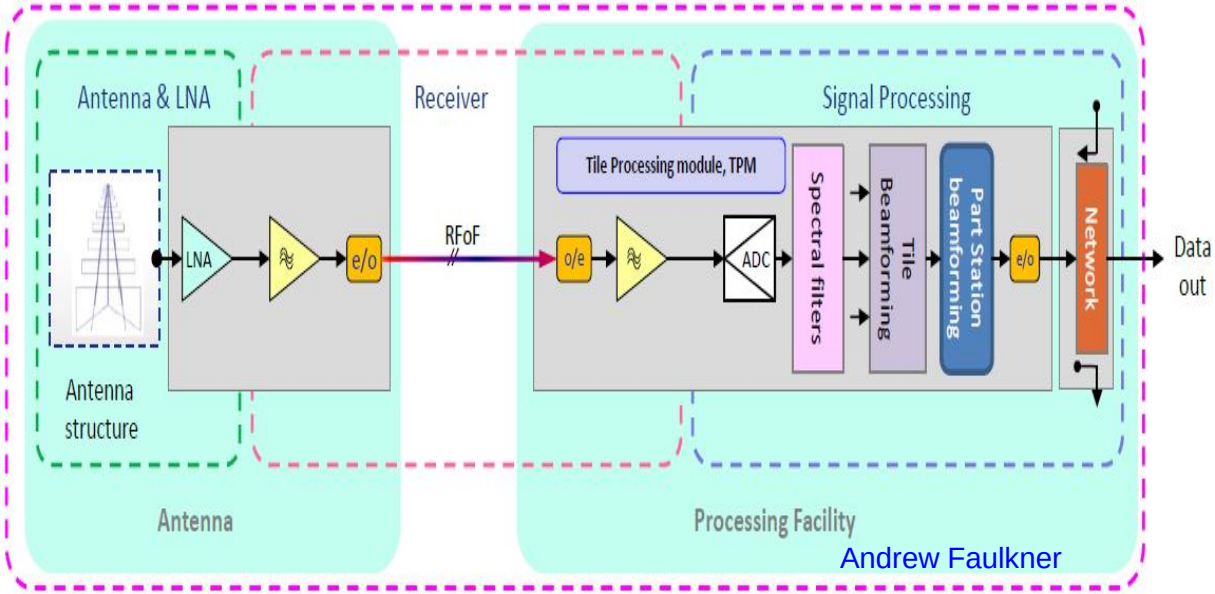
Tile Processing Module

- 16 dual i/p, 14-bit JESD ADCs, AD9680/1Gsps
- Two FPGAs – Xilinx Kintex XCKU040
- Two, 40 GbE Fiber link(QSFP)
- 96-bit wide bus to 1 Giga-by





INAF Italy and collaborators



Challenges of LFAA

- Digitizing 131,072 antennas
- Digital signal processing and modelling
- Tile & Station beamforming
- Large bandwidths
- Large data,Power , Size and Cost
- Mass production, Deployment
- Maintenance, Serviceability
- Remote site conditions

- 1 TPM can handle 1 Tile → 16 dual pol antennas
- 1 station requires 16 TPMs
- 512 stations will have 8192 TPMs
- Current Technology with discrete devices

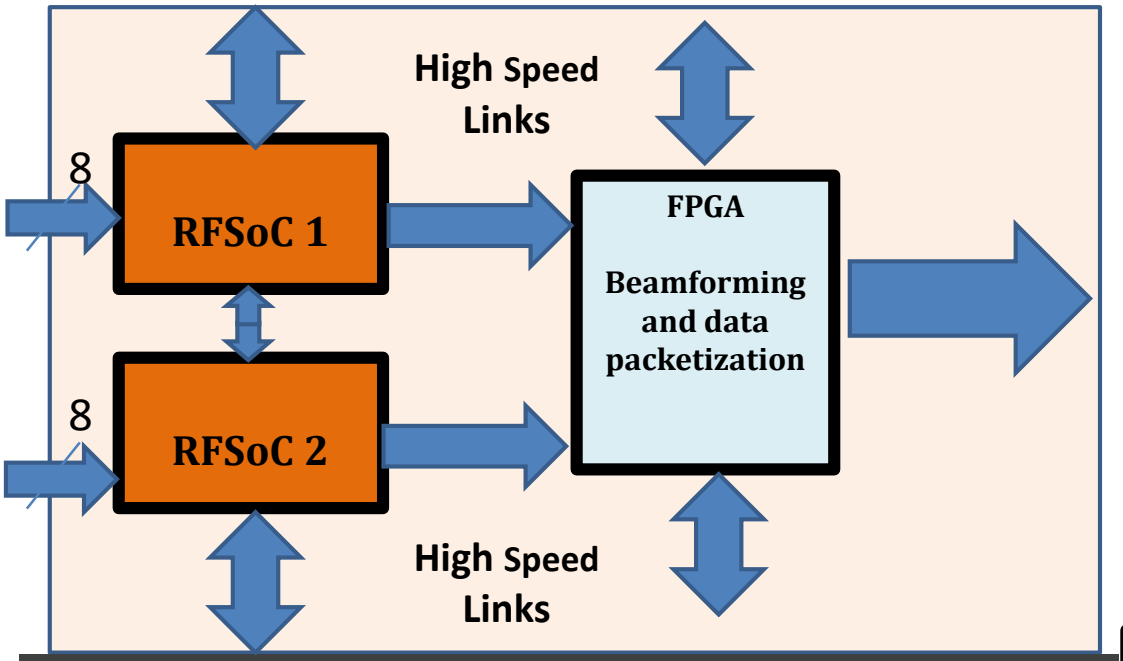
Ref: 2nd URSI AT-RASC, Gran Canaria, 28 May – 1 June 2018

Moving ahead with newer TECHNOLOGY and newer receiver architectures

- Current architecture based on discrete technology -→Size is large , Power is large

Future technology →RFSoC (M-MIMO)

Powerful Combo of 4 technologies
- RF Data converters
- Programmable Logic FPGA
- Processor
- SerDes interface



- Use cutting-edge technology
- Compact design
- PCB design is challenging

- Future technology is RFSoC based Tile Processor
- BIG SAVINGS in Power , Size , Serviceability and Maintenance

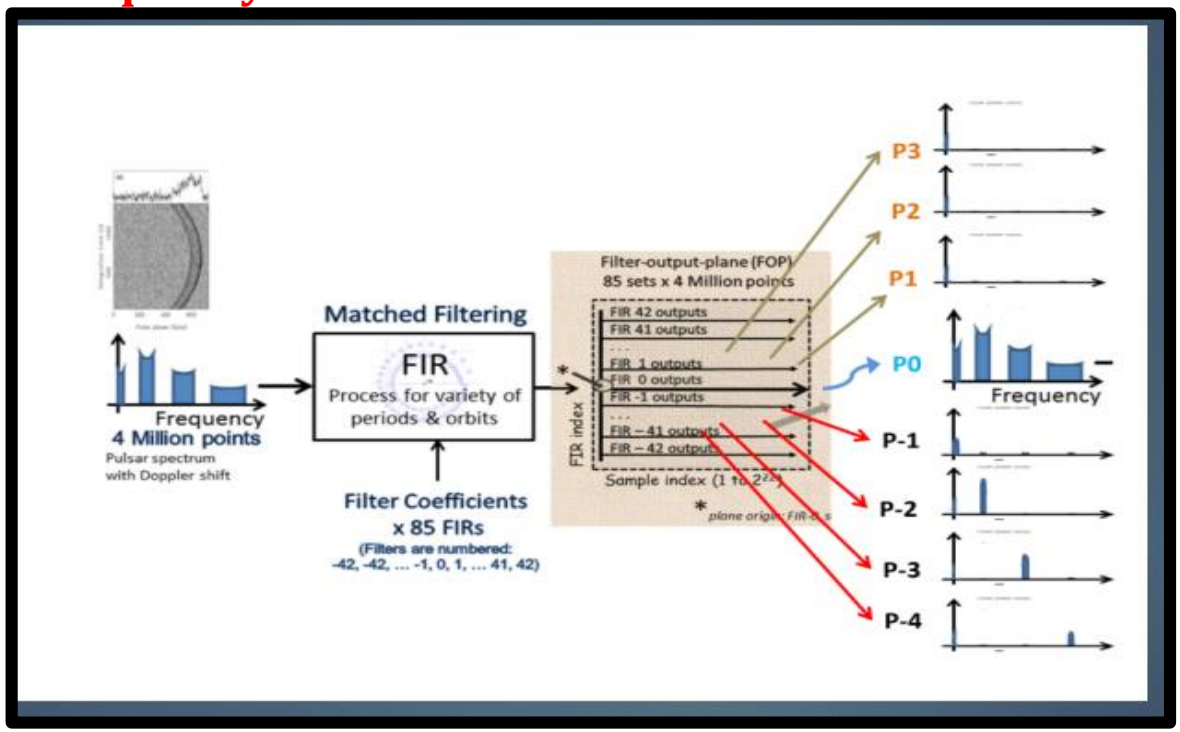
1TPM can handle 1 Tile

One station → 16 TPMs

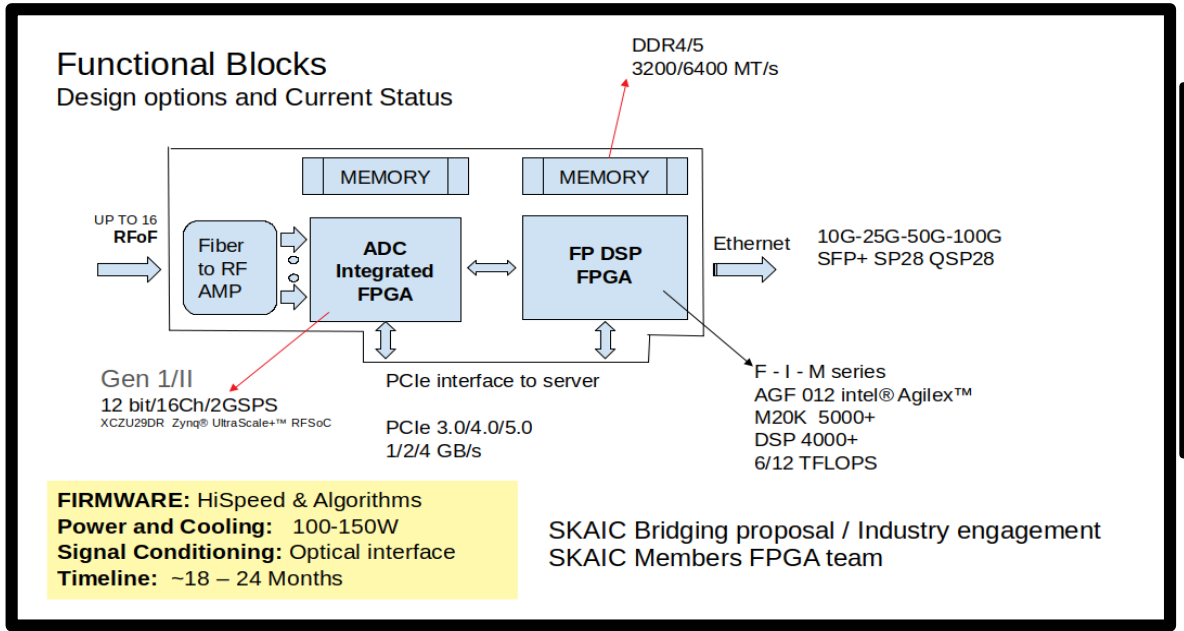
512 Stations will have 8192 TPMs

At RRI : Design and development of RFSoC based Digital Tile Processor

Frequency Domain Acceleration for SKA



- Building the real time pulsar search pipeline for SKA: optimization of algorithms
  - modelling
  - implementation
  - Power performance
- Matched filtering for FDAS
- FPGA implementation along with SKA PSS Team



- Bridging Activity

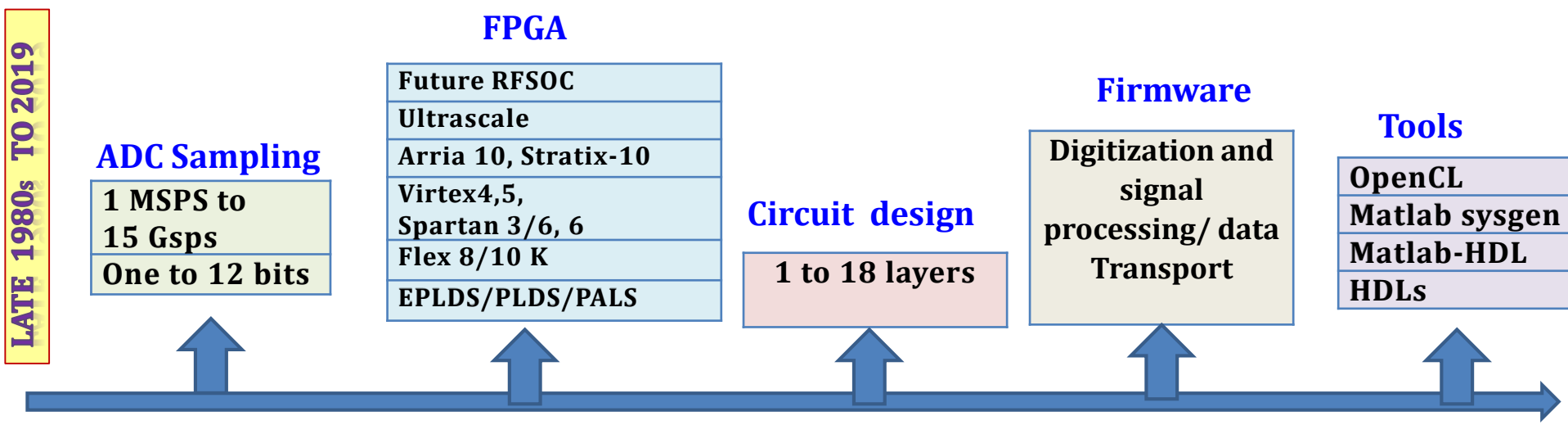
  Development of Accelerator Tile Processor using state-of-the-art RFSoC and floating point FPGAs

  With industry participation

Prabu and SKA PSS Team

SUMMARY

- Relevant expertise, collaboration, industry contacts, infrastructure & capabilities to build high precision, wide bandwidth Digital Receivers
- A collective effort to develop the SWAN with as many as science institutes/universities → realised using Narrow band and Wide band systems
- RFSOC BASED DIGITAL RECEIVERS →
  - Future Technology for Tile Processors for LFAA of SKA, MWA Phase 3
    - RRI is embarked upon development of Future Tile processors



Looking forward for active collaboration and participation in future telescopes : SKA-Low and MWA Phase 3

Acknowledgements:

Electronics Engineering group at RRI
Mechanical Department at RRI
Gauribidanur Observatory

THANK YOU

SWAN Team
DISTORTION Team
MWA Team