OVERVIEW OF DIGITAL SIGNAL PROCESSING SYSTEMS AT GMRT

B. Ajith Kumar

Group Head : GMRT Back-end Systems

ARDRA - 2019

Lonavala, Maharashtra

November 15, 2019

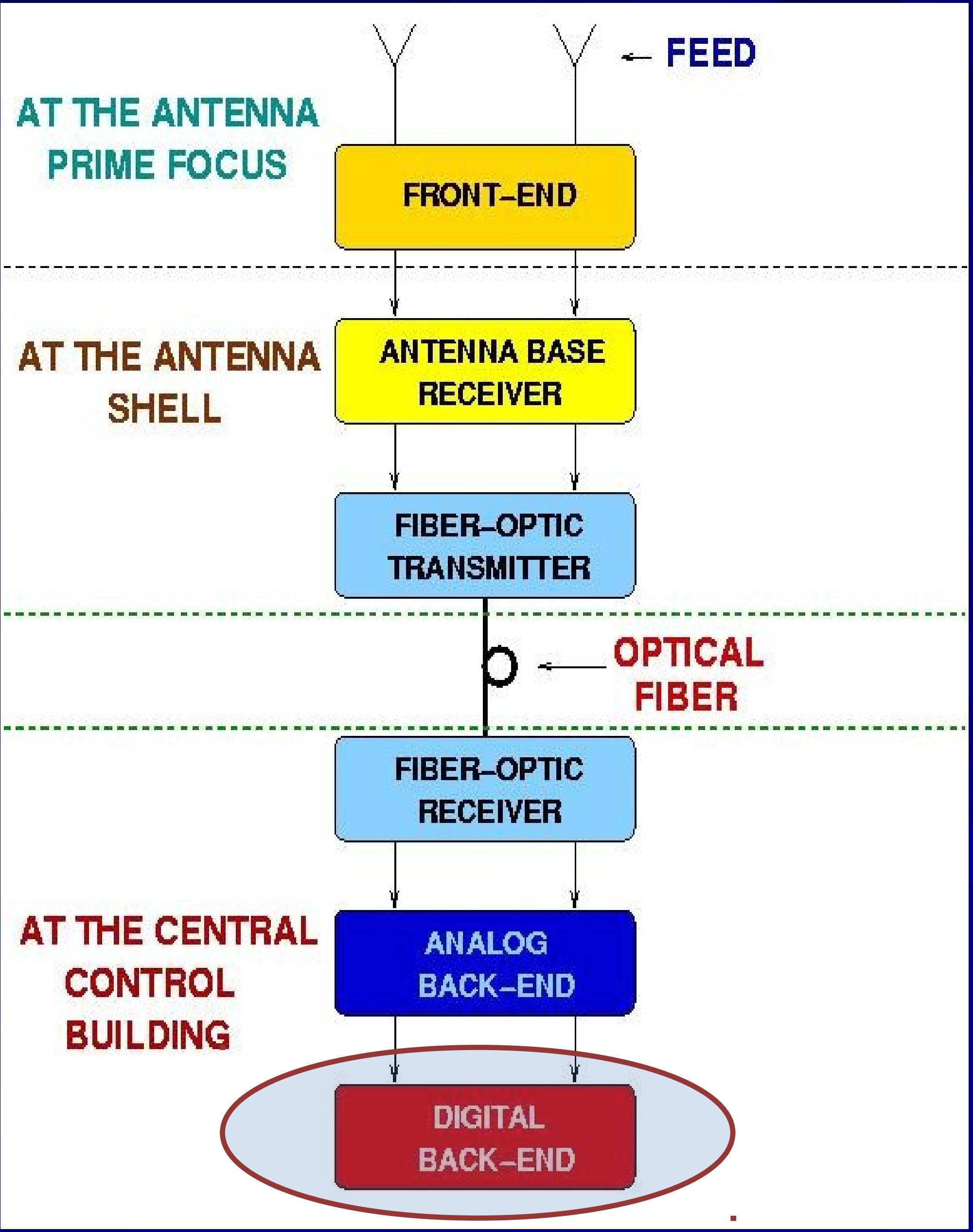
Team Members

- Harshwardhan Reddy : *Signal processing, GPU backends*
- Kaushal Buch : *RFI Filtering, Beamformer for FPAs*
- Sandeep Choudari : *FPGA backends, Walsh scheme*
- Mekhala Muley : *FPGA based signal processing*
- GJ Shelton : *Computing and Networking Hardware*
- Sanjay Kudale : *Data Acquisition, Programming*
- Irappa Halagalli : *Backend system integration & Tests*
- Navnath Shinde : *Time & Frequency Standards*
- Sweta Gupta : *Analog Signal Processing*

Upgraded GMRT

Hybrid Digital Backends

uGMRT Receiver



GMRT Operating Freq : 100 to 1500 MHz

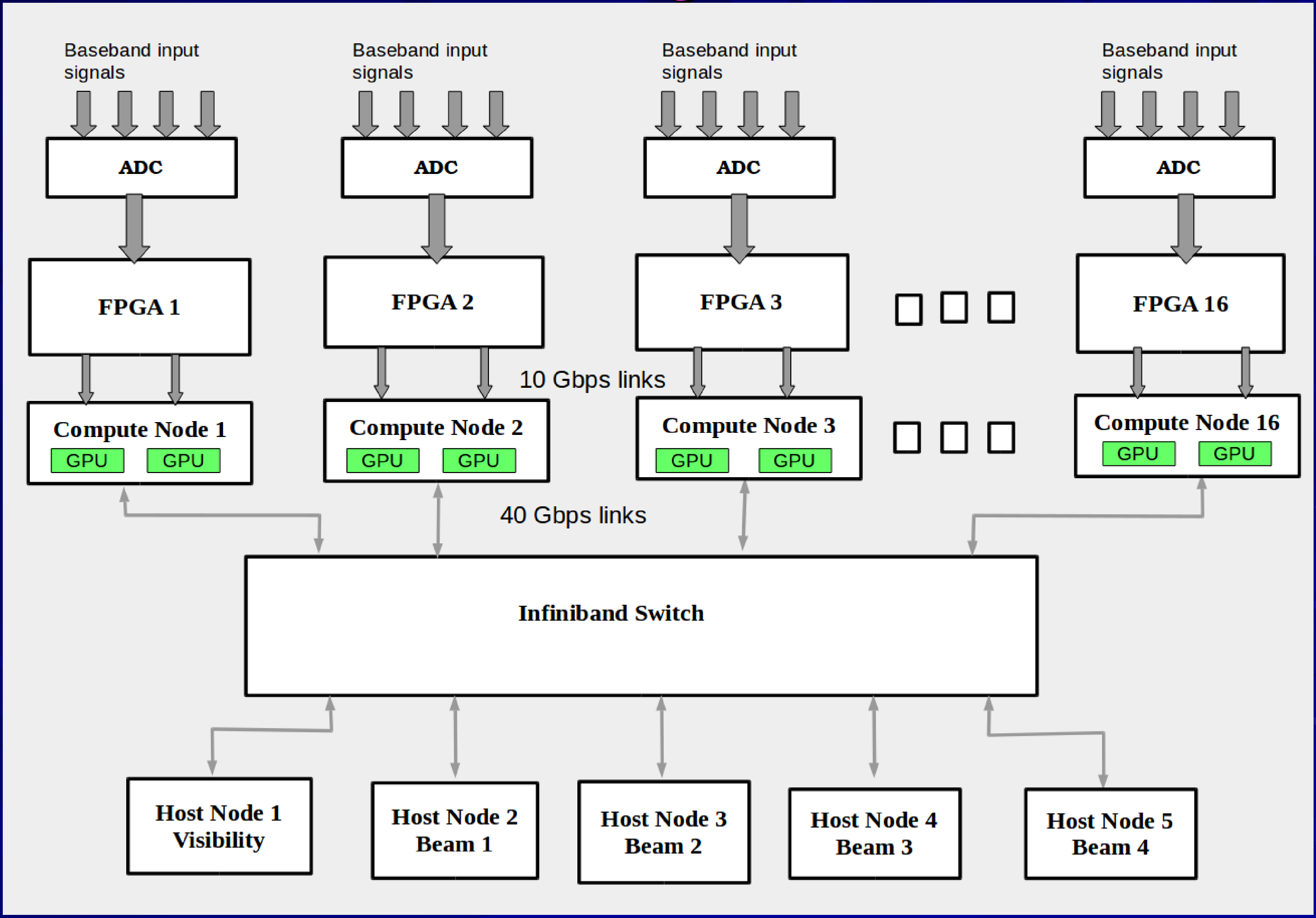
Instantaneous Bandwidth : 400 MHz (max)

Real-time Backend processing to generate Visibility & Beam outputs

uGMRT Backend Specifications

- Number of stations : 32
- Number of input polarizations : 2
- Max instantaneous BW : 400 MHz
- Number of spectral channels : 2048 - 16384
- Full Stokes capability : Yes
- Dump time : 671 ms
- Sub-array support : Yes
- Narrowband modes : Yes (min resolution 95 Hz)
- Number of Beams : 4 (IA or PA or Voltage)
  (max 1 Voltage beam @ 200 Mhz BW)

Design



Baseband input signals
Baseband input signals
Baseband input signals
Baseband input signals
ADC
ADC
ADC
ADC
FPGA 1
FPGA 2
FPGA 3
FPGA 16
10 Gbps links
Compute Node 1
GPU
GPU
Compute Node 2
GPU
GPU
Compute Node 3
GPU
GPU
Compute Node 16
GPU
GPU
40 Gbps links
Infiniband Switch
Host Node 1 Visibility
Host Node 2 Beam 1
Host Node 3 Beam 2
Host Node 4 Beam 3
Host Node 5 Beam 4

GWB : Compute Requirements

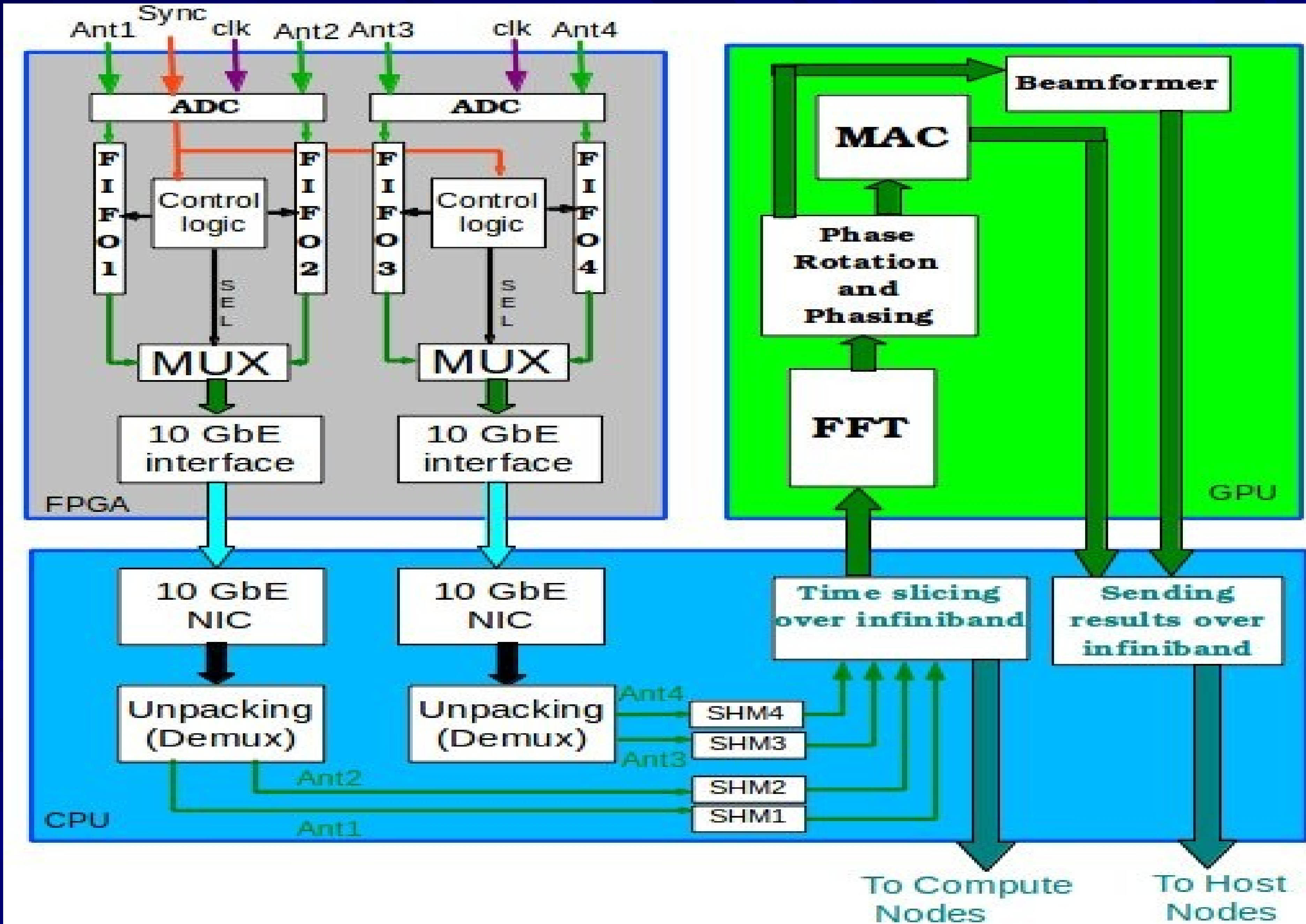
Bandwidth	400 MHz
FFT	3.1 Tflops (16K)
Phase Shifter	100 GFlops
Multiply & Accumulate	6.4 TFlops
Beamformer	150 Gflops / beam
Total	**10 TFlops**

I/O Data rate :

Input : FPGA board to Compute Node = 12.8 Gbps
Sharing : Compute nodes = 12 Gbps (bidirectional)

Visibility Output = 3.2 Gbps (16K spectral channels Total Intensity)
Beam Output = 1.6 Gbps (PA Total Intensity at 20 uS)
Voltage beam Output = 6.4 Gbps

Data Flow in single FPGA-GPU



Hardware Implementation

16 ROACH (FPGA) boards with Atmel/e2v based ADCs developed by CASPER group for digitization & packetization

16 Dell T630 machines as Compute Nodes

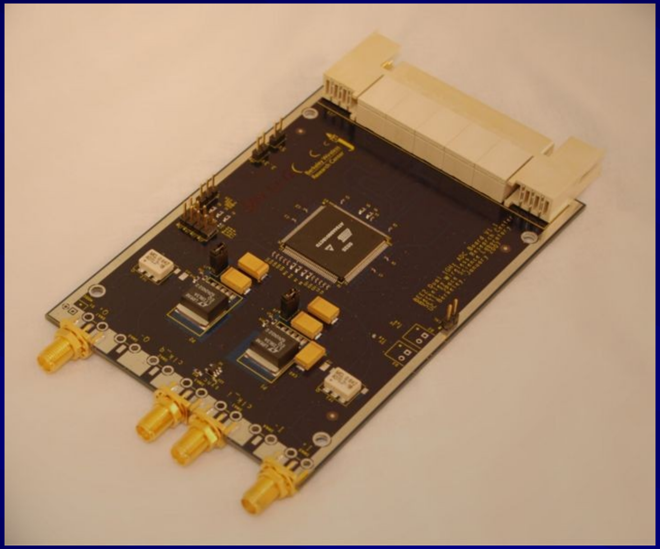
32 Tesla K40c GPU cards for processing

Dell servers as Hosts : Visibility-1, Beam-4

36 port Mellanox Infiniband switch for data sharing between Compute Nodes and Host Nodes

Developed in collaboration with Swinburne University, Australia

GMRT Backends : Hardware Components



<u>CASPER design</u>
ADC board (iADC)
ADC Chip : Atmel/e2v
8-bit Dual ADC
Max. clock : 1.2 GSps
Analog BW : 1.5 GHz

<u>CASPER design</u>
FPGA Virtex 5 boards
RAM : 512 MB DDR2
AMCC PowerPC
2 Z-DOK connectors
4 CX4 10Gbps conn.

GMRT Backends : Hardware Components

<u>Compute node Dell T630</u>

Processors : 2 x Intel Xeon E5-2600 v4
RAM : 64 GB DDR4 DIMMs
Drive Bays : 32 x 2.5" or 18 x 3.5"
PCIe slots : X 8 slots
GPU Support : Four GPUs 300W
Embedded NIC : Dual port 1 GbE

<u>GPU : nVidia K40</u>

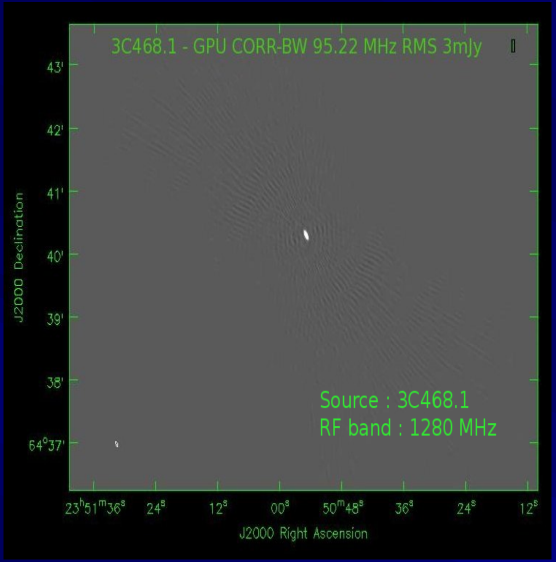
No. of cores : 2880
Global memory : 12 GB
Memory bandwidth : 288 GB/s
Board Power : ~235 Watt
No. of Multiprocessors : 15
Peak performance (SP) : 4.29 Tflops
Peak Performance (DP) : 1.43 Tflops

GMRT Backend implementation

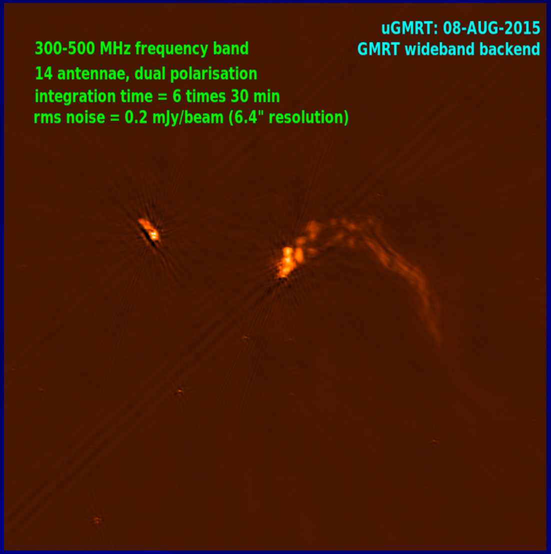
Compute Nodes

Host Nodes

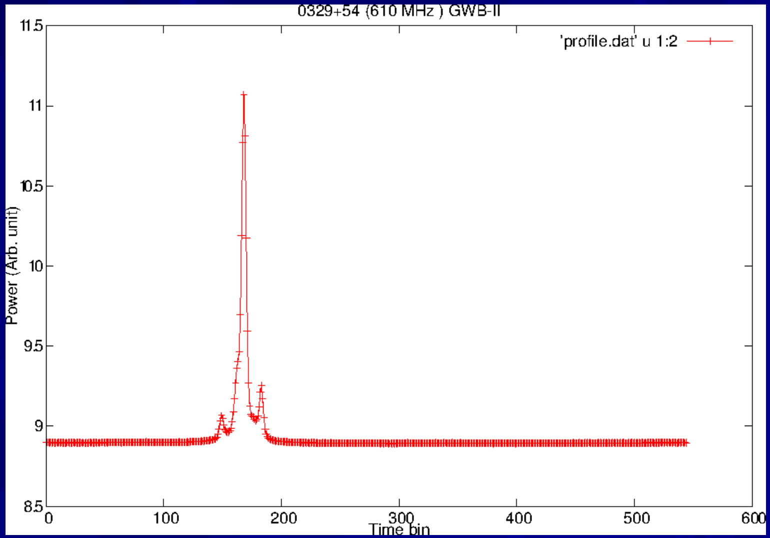
Typical Results - uGMRT



First image using GWB
Source 3C468
L-band, 100 MHz BW
RMS noise – 3 mJy



Source : 3C129
14 antennas, 300-500MHz
Bandwidth : 200MHz



Pulsar : B0329+54
8 antennas, IA mode
RF : 610 MHz

Image Courtesy : DV Lal & Others

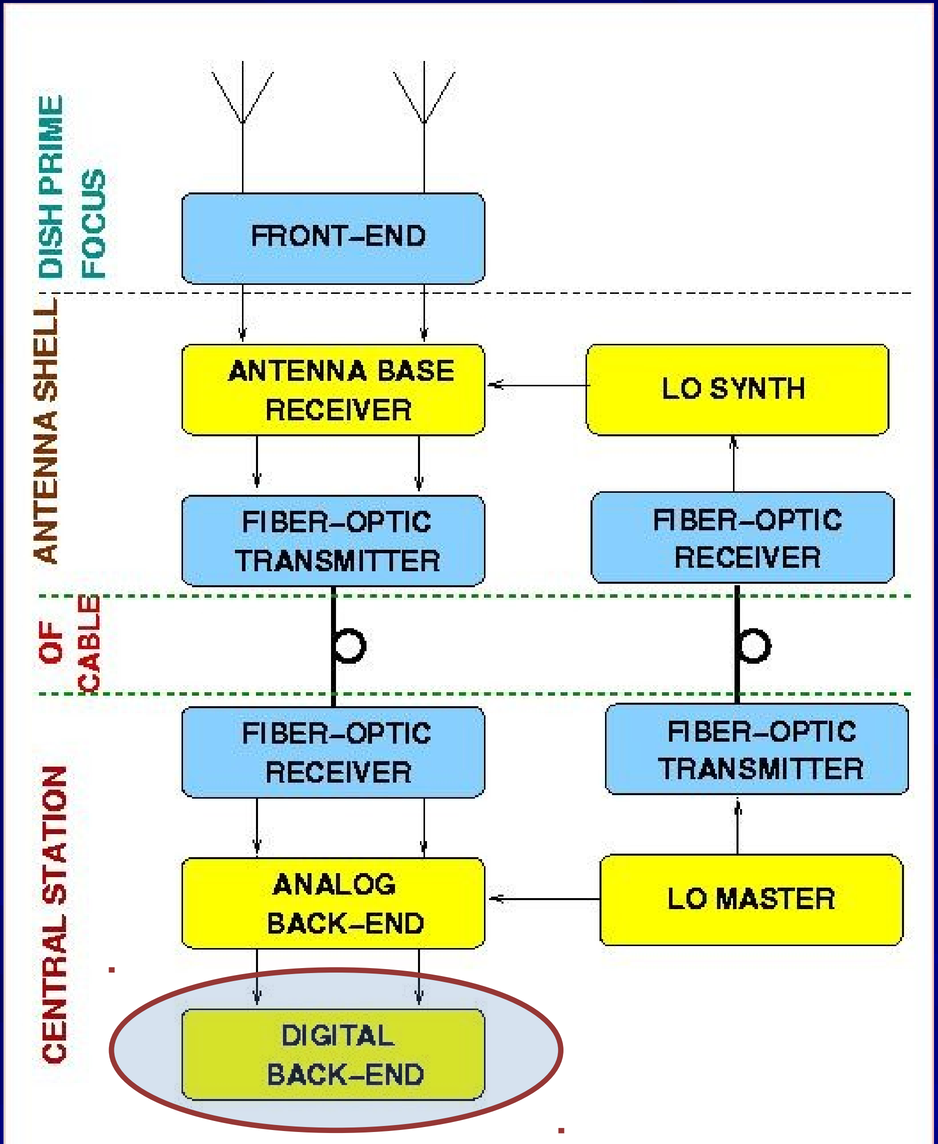
GWB Current developments

- User host for data access by Telescope user during observation
- Implementation of PFB for channelisation & narrow band modes
- Parallel Backend System - GPB for raw voltage record + process
- Tests on new servers and GPUs for next level update
- Prototype tests on Early digitisation at Antenna site

GMRT

Software Backends

GMRT Receiver



GMRT Operating Freq : 100 to 1500 MHz

Instantaneous Bandwidth : 32 MHz (max)

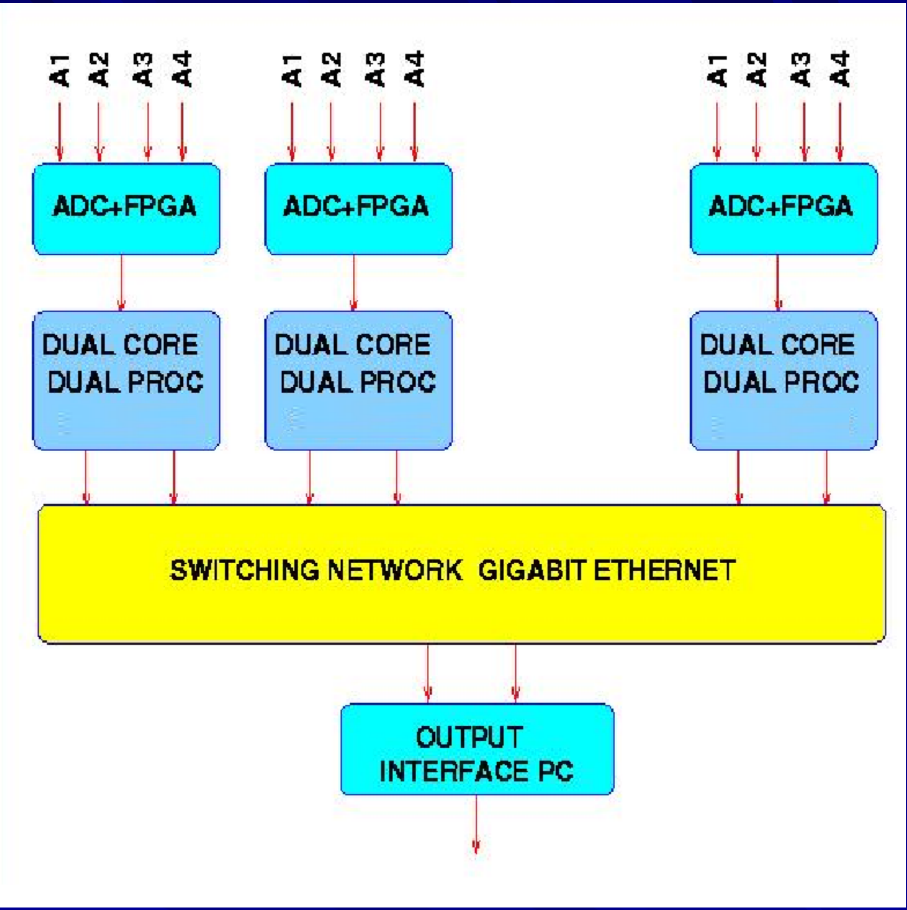
Real-time Backend processing to generate Visibility & Beam outputs

GSB specifications

Number of stations	: 32
Number of input polarizations	: 2
Max instantaneous BW	: 32 MHz
Number of spectral channels	: 512
Full Stokes capability	: Yes
Dump time	: 2 s
Sub-array support	: Yes
Narrowband modes	: Yes
Number of Beams	: 2 (IA or PA or Voltage)
Raw voltage recording	: 16 Mhz, 4 bits/sample

Software Back-end

- Digitisation on ADC boards
- Analog signal : 16/32 MHz BW
- ADC to CPU via interrupt driven DMA
- Distribute data to each node time slice
- Delay, FFT, Fringe stop, MAC at node
- Record integrated visibilities results



<u>ACQ Nodes</u> : Dual core, Dual processor Intel Xeon CPUs

With 8-bit, 4 Channel, 66 MSPS, PCI-X compliant ADC card

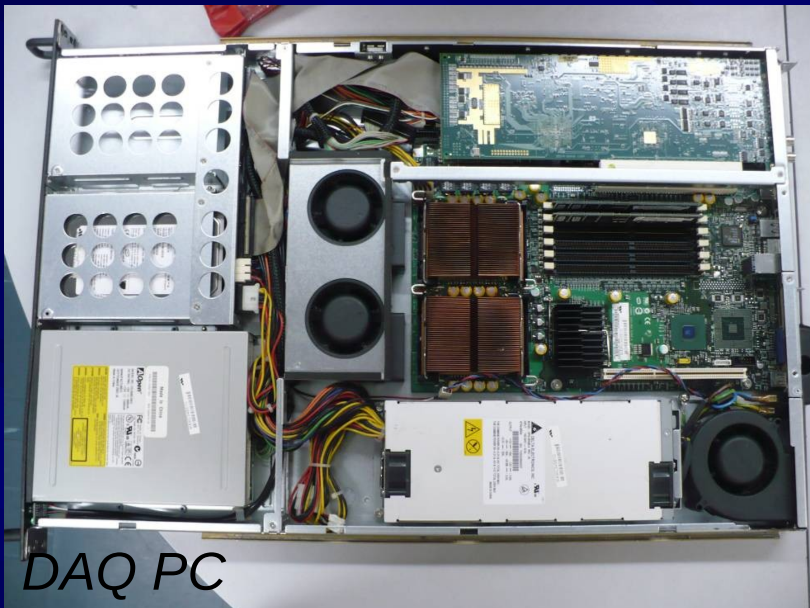
<u>Compute Nodes</u> : Quad core, Dual processor Intel Xeon CPUs

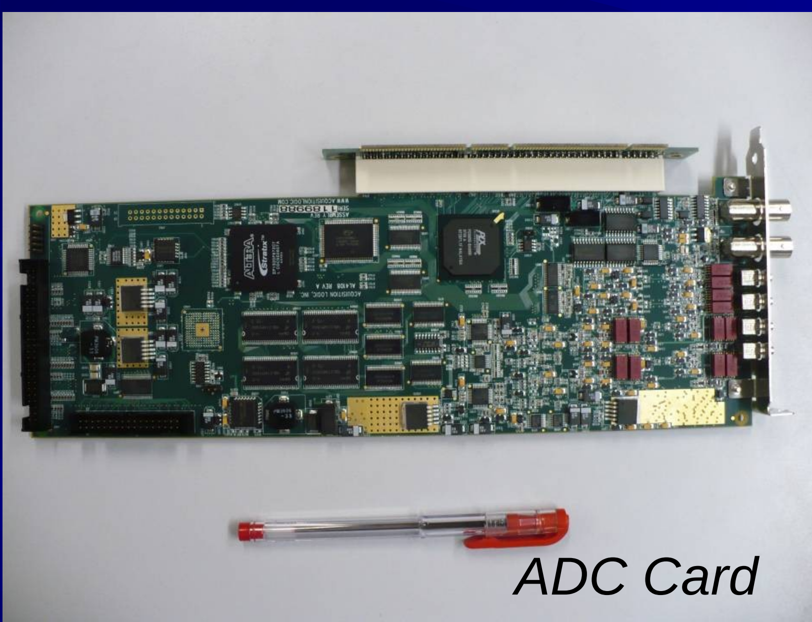
<u>Recording Nodes</u> : Dual core, Dual processor Intel Xeon CPUs

Number of Nodes required = 48

Details from Report : J.Roy+others

Software Back-end Implementation





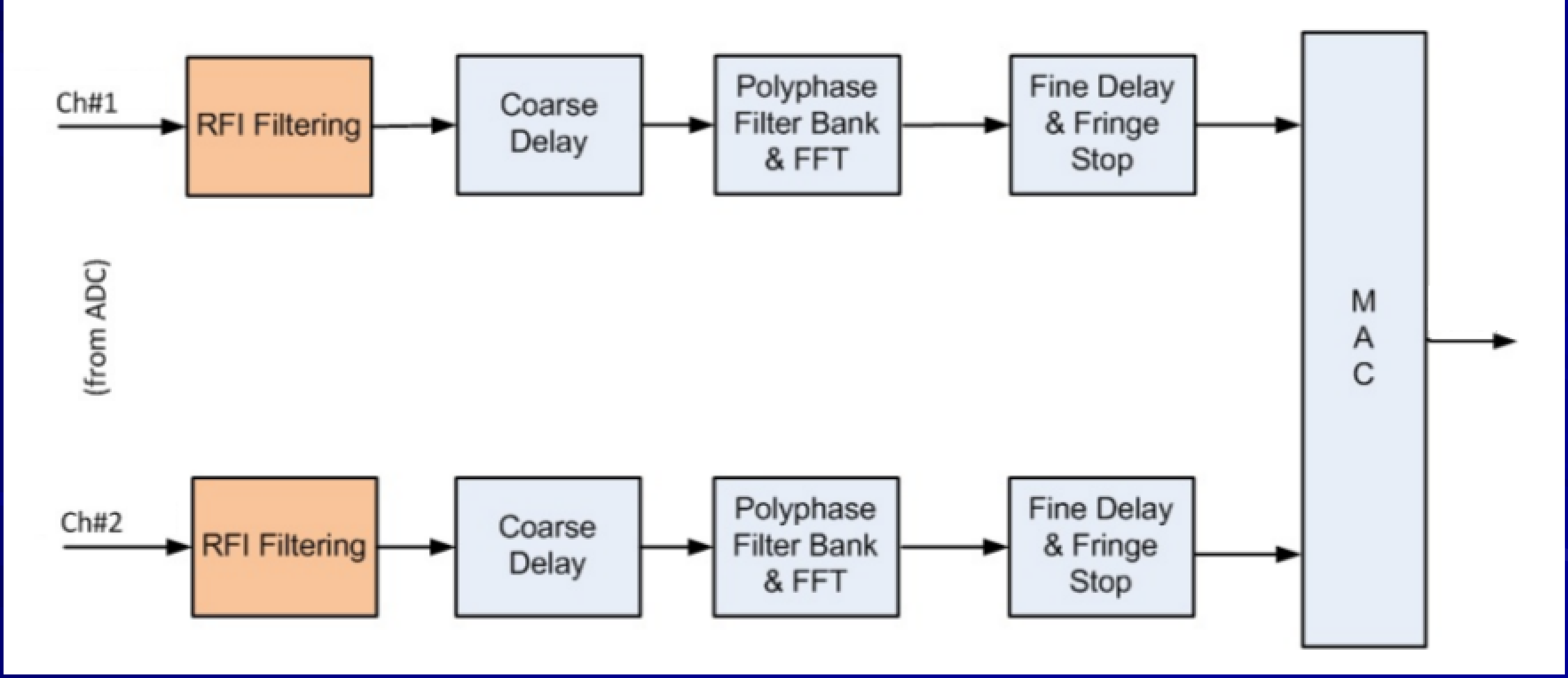
Other CASPER based designs

• Packetised Correlator Packetised Beamformer	: 8 ant, 2 pols, BW 400MHz (Using iADC+Roach boards)
• Pocket Correlator Pocket Beamformer	: 2 ant, 2 pol, BW 400MHz (Single Roach board)
• Design Blocks	: Coarse Delay Fine Delay + Fringe Stop Gaussian Random number gen Impulsive RFI Excision
• 32 mtr dish Backend	: 2 pols, self & Raw-data (Single iADC+Roach)
• 15 mtr dish Backend	: 2 pols, self & Radata (Single iADC+Roach)
• Digital Noise Generator	: 2 outputs with variable corr (Single Roach Board)

Recent Developments

RFI Mitigation for GWB

Broadband RFI detection and cancellation scheme developed.
The scheme uses the statistical properties of astronomical signal.
Implemented in the digital backend on FPGA boards.



Real-time RFI Detection and Filtering

Median Absolute Deviation (MAD) is a robust measure of dispersion of data set.

MAD = median (abs (Xi – median(X)))

Standard Deviation = 1.4826 X MAD

Threshold = [median ± n*σMAD]

Real-time calculation of Standard Deviation of data set.

RFI detection by comparing with Threshold.

Filtering options - replacement with

1. Constant value 2. Digital noise 3. Threshold

To take care of longer bursts of RFI, Median of MAD (MoM) is used,

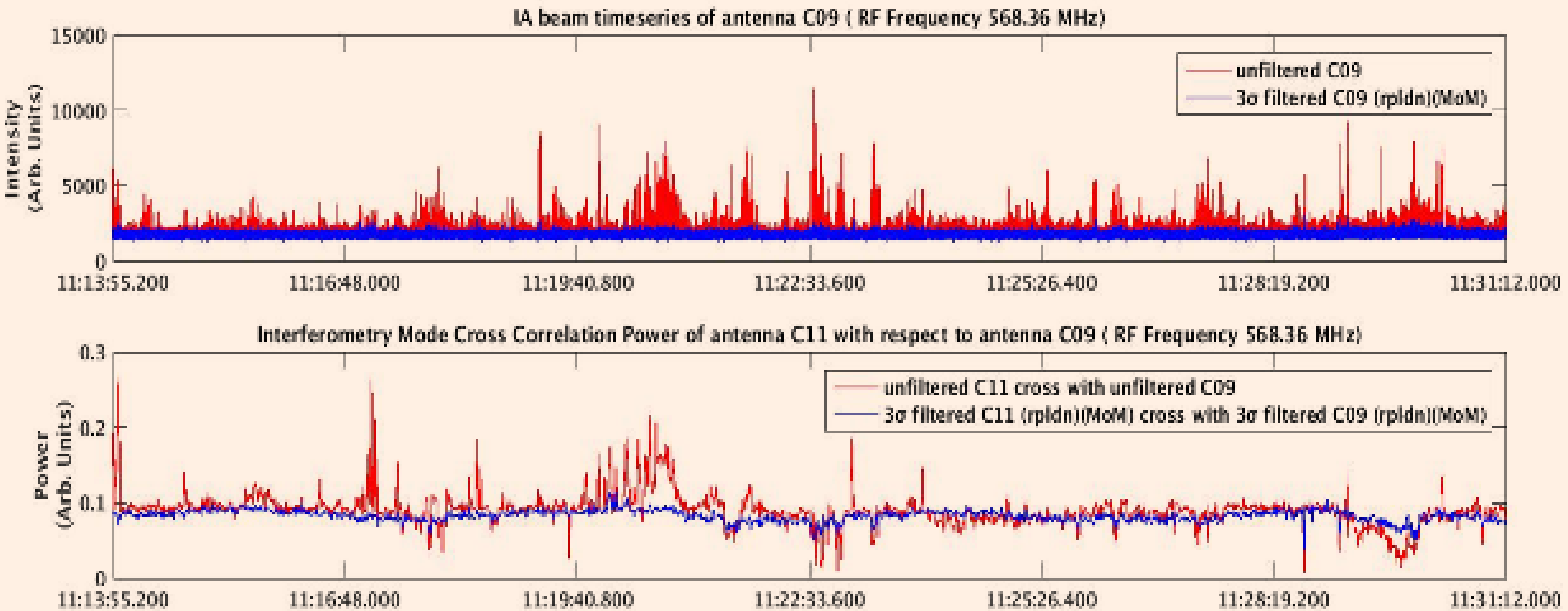
Median of MAD (MoM) = M(D1, D2, ... , Dn)

The current design uses 16k MoM – i.e. median of 16k MAD values.

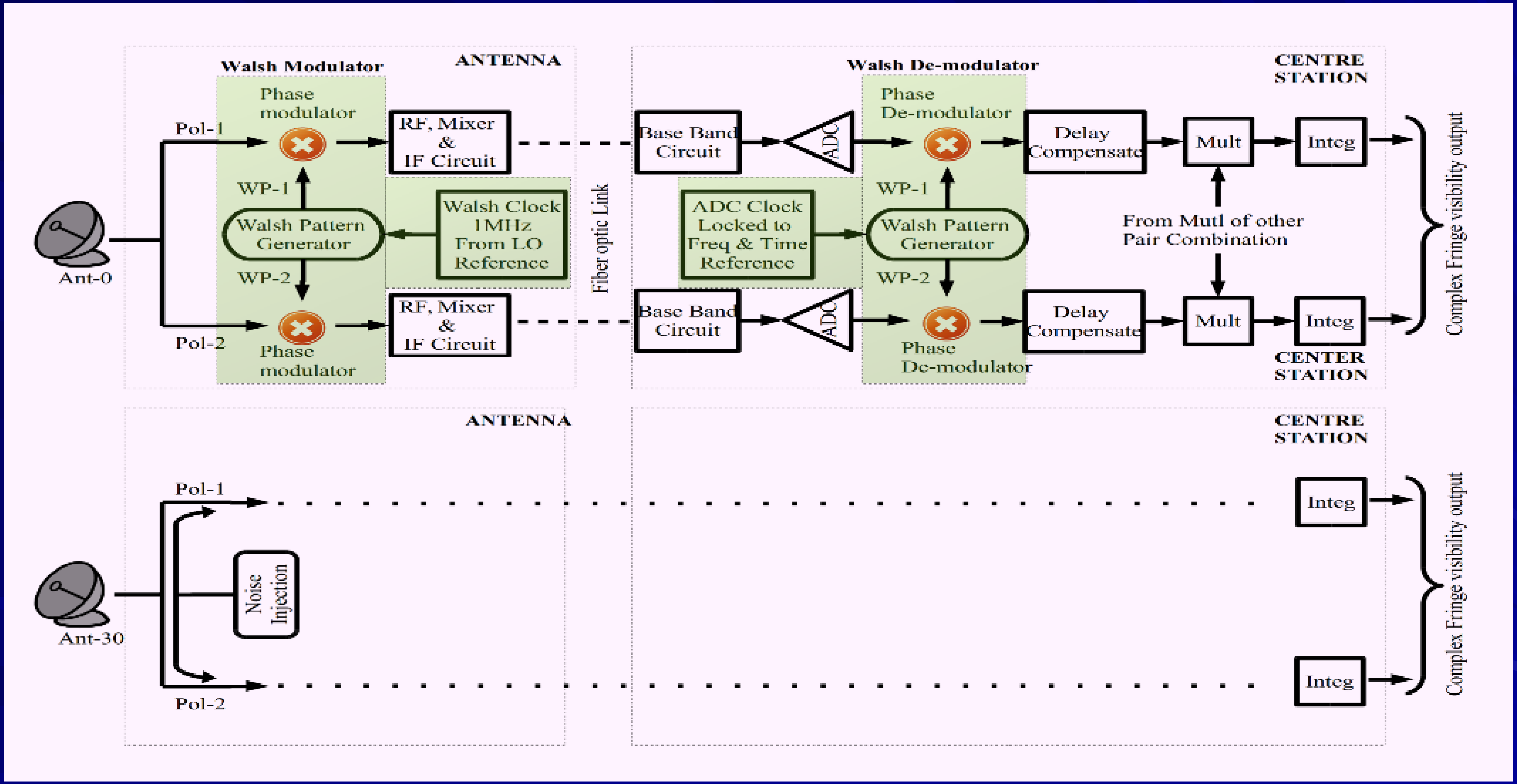
RFI counter keeps record of number of detected RFI samples and total samples.

Test Results – RFI Filtering

- Effect of RFI filtering on Beam output and visibility output
- Tested using two closely spaced antennas, C9, C11



Walsh Scheme for GMRT

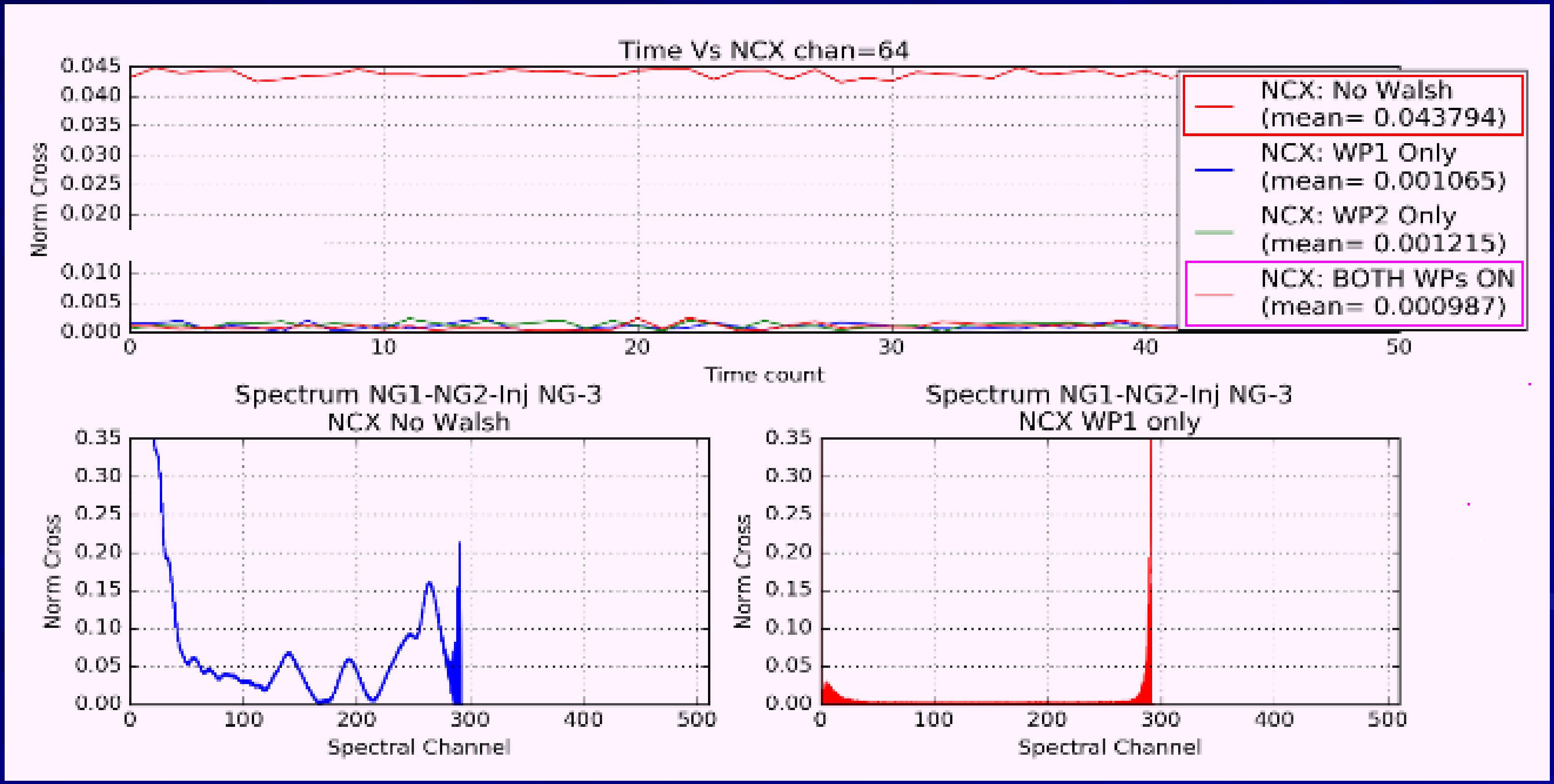


Walsh modulation scheme

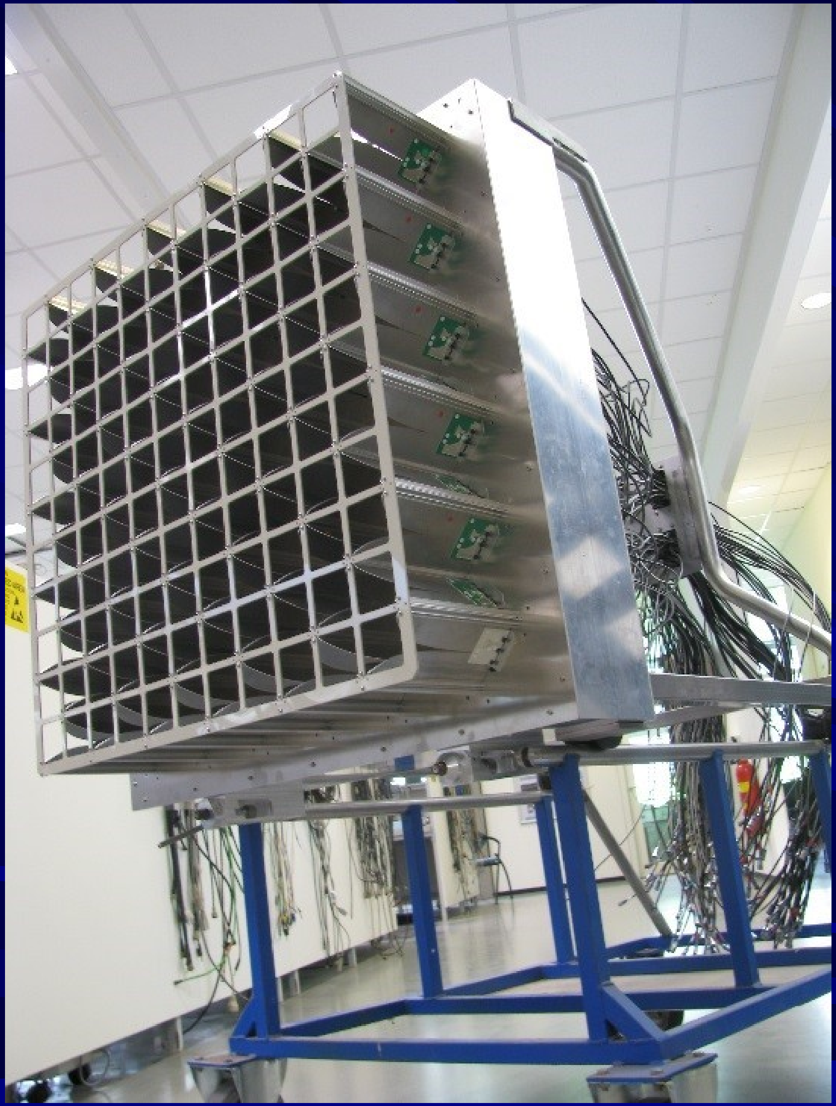
- 128 bit Walsh pattern used at GMRT
- 64 unique patterns for Phase modulation of RF signal at antenna
- CPLD based circuit at antenna base for pattern generation
- Sequency Pulse to indicate first bit of Walsh pattern
- Sequency transmitted to central station over return link
- Walsh regenerated at central station in FPGA for demodulation
- Walsh demodulation implemented in Roach board

Results : Cross Talk rejection

- Measured by injecting a common noise to two inputs of GWB
- With no Walsh applied shows a cross corr value of 0.044
- With Walsh in one or both channels cross corr drops to 0.001



Multi-beam Beamformer for FPA

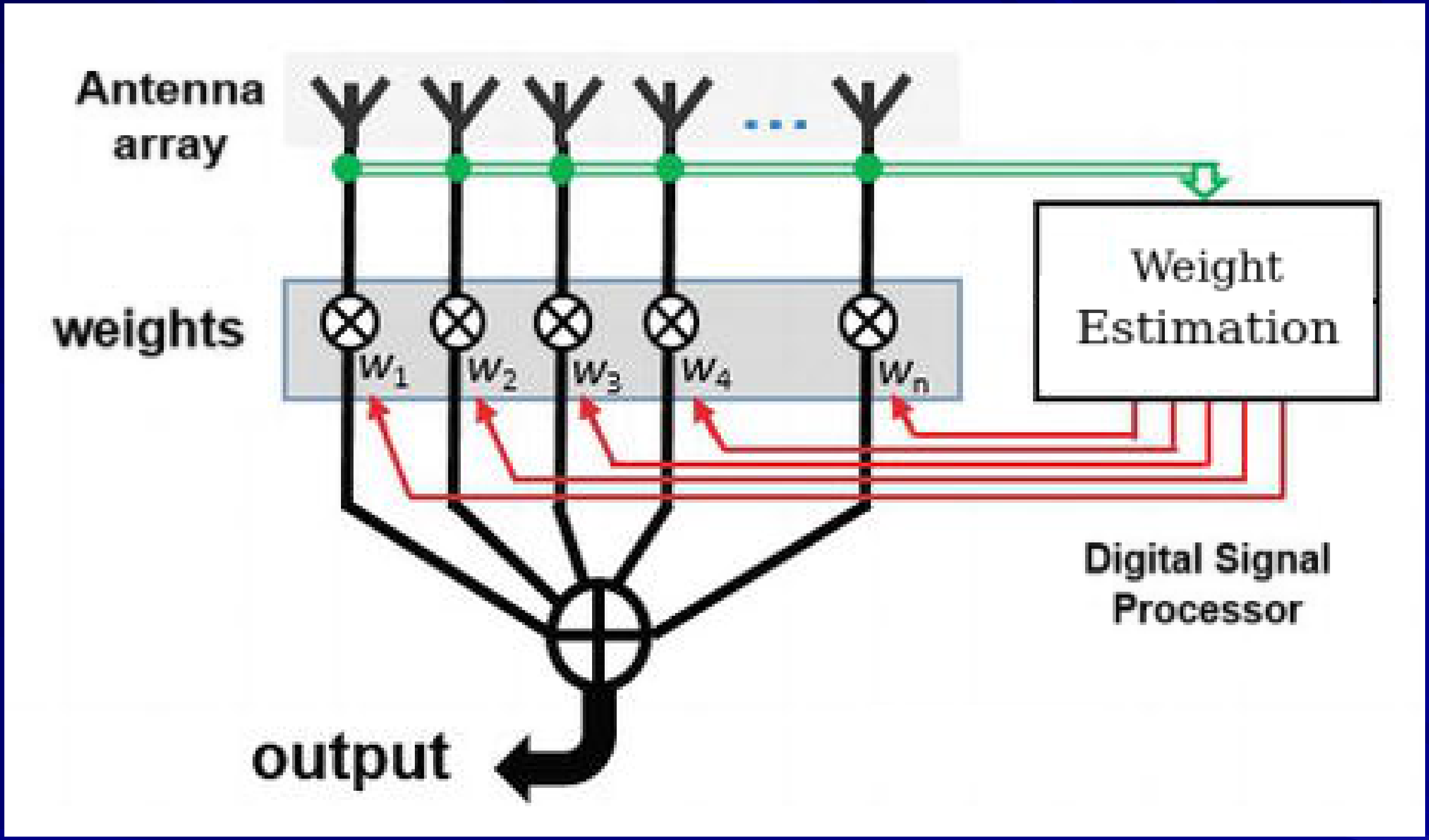


<u>Focal Plane Array</u>

Frequency : 1100 to 1700 MHz
No. of Elements : 8 X 9 dual pol
Vivaldi Elements : Aluminium
Element spacing : 11 cm

FPA unit developed by Astron
Tech Info Courtesy : Astron Documents

Beamformer

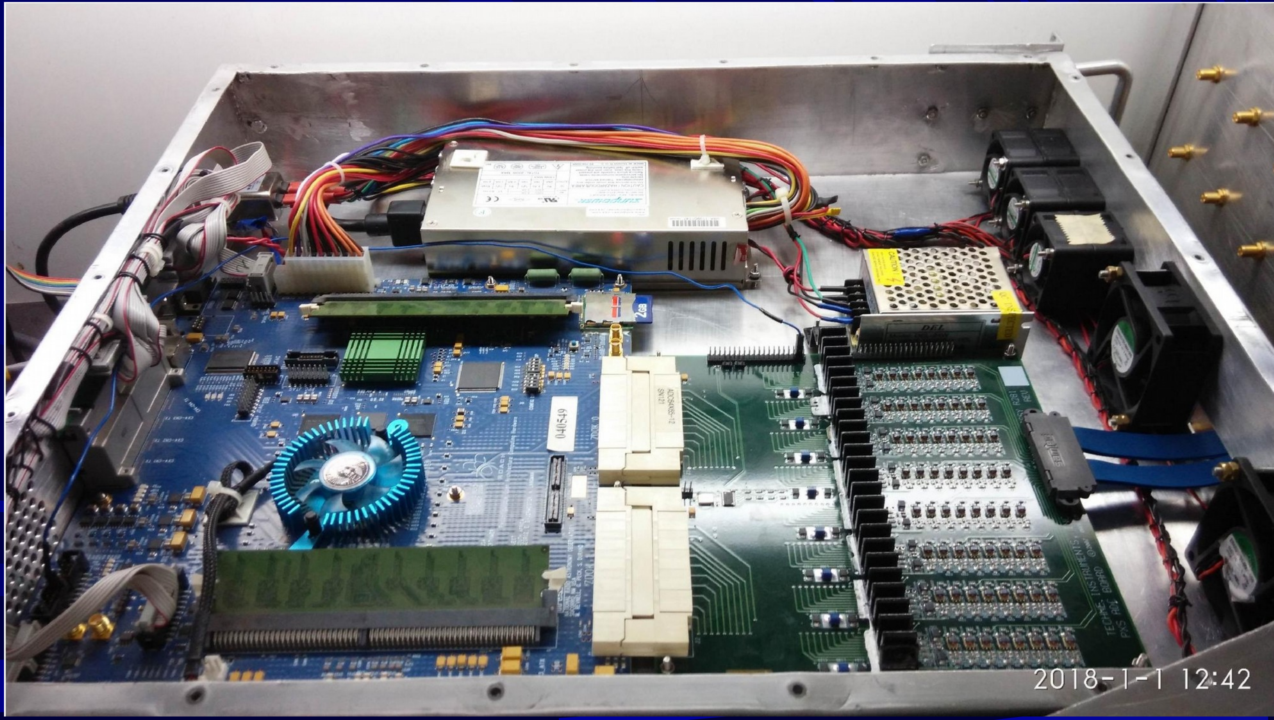


Beamformer Hardware : 64-input, 12-bit ADC connected to ROACH board
Narrowband multi-beam beamformer & correlator (max. 32 MHz bandwidth)

Beamformer - Implementation

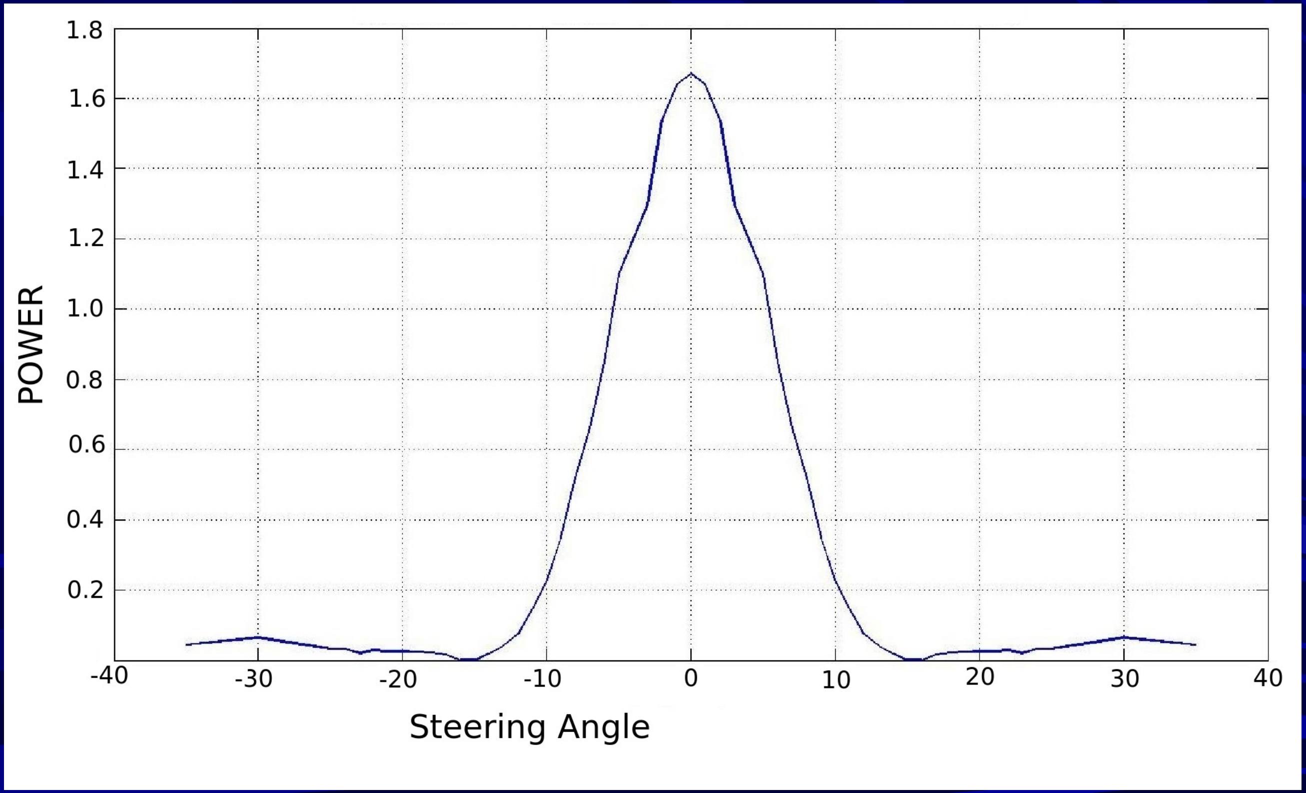
Beamformer

Bandwidth : 32 MHz
Beam former : 16 inputs, 4 beams
Freq resolution : 31.25 Khz, 1024 Ch
Phase scaling : 360 deg mapped to 2048
Amp scaling : 8 unsigned bits - 24 dB
Integration time : 0.671 s
Beam power : 16 bits



Beam Steering

1. 8 elements used for testing the Beam steering
2. A CW signal transmitted using the 3 mtr dish
3. Beam formed with appropriate weights applied to each element
4. The beam is steered in a vertical direction by changing the phase.




Thank You ...